INTEGRATED ELECTRONICS DESIGN FOR HIGH-FREQUENCY INTRAVASCULAR ULTRASOUND IMAGING

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Gokce Gurun

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INTEGRATED ELECTRONICS DESIGN FOR HIGH-FREQUENCY INTRAVASCULAR ULTRASOUND IMAGING

Approved by:

Dr. F. Levent Degertekin, Co-advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Paul Hasler, Co-advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Maysam Ghovanloo
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Pamela T. Bhatti
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Thomas E. Michaels
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Ajit Yoganathan
School of Biomedical Engineering
Georgia Institute of Technology

Date Approved: October 6, 2011

To the everlasting love and support of

my Mom, my Brother and

my Wife…

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SUMMARY

Intravascular ultrasound (IVUS) imaging has emerged as a valuable tool for interventional cardiology to manage coronary artery disease, the leading cause of death in the U.S. One limitation of the existing IVUS systems is that they cannot generate volumetric images viewing directly in front of the catheter, which would be an invaluable clinical capability for guiding interventions. In addition, currently there are no IVUS array systems operating at high-frequencies (above 30 MHz), which is a shortcoming that prevents achieving the resolutions needed for early detection of atherosclerotic disease.

For successful realization of next-generation navigational and diagnostic IVUS imaging tools that can address these limitations, close integration of custom-designed front-end electronics and the transducer array within the catheter is very critical. Therefore, this research aims to develop and implement custom-designed electronic circuits and systems integrated with an IC compatible capacitive micromachined ultrasound transducer (CMUT) technology for realization of these miniature IVUS imaging catheters operating at 10-50 MHz frequency range.

This research showed that it is possible to implement all of the required front-end electronics in a single IC that can get monolithically integrated with the CMUT array (CMUT-on-CMOS) to realize a single-chip, highly-flexible forward-looking (FL) IVUS imaging system. Single-chip integration is very advantageous as it minimizes the parasitics, reduces the manufacturing complexity significantly and enables the ultimate miniaturization of the catheter. The custom-designed IC fits into a very small (1.5-mm diameter) donut shaped area to be suitable for operation within a tiny vessel and

consumes less than 20 mW. Successful implementation of the single-chip FL-IVUS system is demonstrated through volumetric imaging experiments.

The CMUT element size in a FL-IVUS ring array is very small with dimensions on the order of 100 μm limiting the available signal levels. Therefore, to maximize the SNR, it is critical to custom design receive amplifiers to minimize the electronics noise. In this work, the transimpedance amplifier that is custom-designed in 0.35-μm CMOS process achieved CMUT thermal-mechanical noise (T-M) dominated receive performance with a noise figure of 1.8 dB in a CMUT-on-CMOS implementation. This research also showed that the transducer T-M noise dominated detection system can be used as an effective tool for CMUT array characterization and also as an enabling method for new sensing and imaging applications.

The high-frequency IVUS imaging application requires a power and area efficient implementation of a high-frequency dynamic receive beamforming circuitry inside the catheter. In this research, to perform the delays, a current-mode all-pass-filter-based analog delay cell that can generate dynamically variable delays at high frequencies is developed. A biquad current mirror is explored as a method to extend the bandwidth of the delay circuitry by a factor of 6. A dynamic receive beamformer IC based on the developed delay cell is designed in a 0.35-μm CMOS process for monolithic integration with an annular CMUT phased-array. The overall power consumption of the IC is small enough (~70 mW) for safe operation within a catheter. The fabricated beamformer IC was successfully connected to a CMUT annular array and the desired preamplification and dynamic receive beamforming capabilities of the IC are demonstrated.

CHAPTER 1

INTRAVASCULAR ULTRASOUND IMAGING

Medical ultrasound imaging is a well-established and widely used diagnostic tool in modern medicine. It is relatively inexpensive and portable compared to other imaging techniques such as magnetic resonance imaging (MRI) and computer tomography (CT). It is also considered to be a safe tool as it uses non-ionizing radiation. The most well-known application of ultrasound is its use in monitoring the fetus in the womb. Medical ultrasound is also used for real-time imaging of the cardiac structures, the vascular system and abdominal organs; and to map tissue motion and blood flow in liver and heart. In addition, it is also used in therapeutic applications, such as targeted drug delivery and treatment of breast cancer; and in nondestructive testing to find flaws in materials and to measure the thickness of objects [1].

Although ultrasound refers to frequencies above 20 kHz, which is the hearing threshold of the human ear, conventional medical ultrasound systems targeted at imaging the heart or abdominal organs typically use frequencies ranging from 1 MHz and 10 MHz. On the other hand, ultrasound imaging at higher frequencies (as high as 45 MHz) has been used and proposed in applications that require a better image resolution, such as dermatology, small animal, and intravascular imaging. This dissertation concentrates on the use of high frequency medical ultrasound particularly for catheter-based imaging. The motivation for use of intravascular ultrasound for detection and diagnosis of coronary diseases is discussed in the following section.

1.1. Intravascular Ultrasound (IVUS) Imaging and Its Clinical Use

Coronary heart disease kills more people than any other form of disease. In 2008, an estimated 7.3 million people died of coronary heart disease worldwide [2]. This disease is caused by atherosclerosis, which occurs when the coronary arteries that carry oxygen and nutrient-rich blood to the heart muscle become narrowed or blocked due to buildup of cholesterol and fatty deposits (plaque) in the arteries. It is a syndrome restricting adequate blood flow to the heart, which is likely to lead to serious heart problems including angina pectoris (chest pain) and heart attacks.

Since the 1960s angiography has been the predominant way of evaluating plaque buildup (atheroma) inside the coronary arteries. In coronary angiography, a catheter is inserted into the vessel to inject a contrast agent into the blood vessel close to the desired area to be visualized. The contrast agent becomes visible in the X-ray imaging by absorbing the x-rays and enables to visualize the lumen (opening) of the arterial wall. Diagnosis of coronary heart disease is made based on whether any severe stenosis (narrowing of the arterial opening) is found compared to the diameter of a "normal" segment.

Although, angiography has been widely used and is a very valuable imaging modality, it has several important limitations. First of all, angiography can only detect plaque buildup at areas with severe stenosis that significantly narrows the arterial opening and limits the blood flow. However, at early stages of the formation of the plaque, the vessel wall remodels, and plaque buildup gets confined within the arterial wall without resulting in any arterial narrowing. This conceals the early plaque buildup on angiography [3]. Clinical studies revealed that most coronary syndromes, in fact, develop

in territories with early plaque buildup and with minimal arterial narrowing which look like mild, insignificant lesions in the coronary angiography. Therefore, angiography often can misdiagnose a diseased vessel as “normal” [4] and is not strongly reliable in the early diagnosis of the coronary heart disease. In addition, the estimation of stenosis based on the angiograms has significant observer variability approaching 50% [5].

Recently, intravascular ultrasound (IVUS) imaging has emerged as a valuable imaging modality for interventional cardiology for the effective diagnosis and assessment of the extent of coronary artery disease [6-9]. In IVUS imaging, a long, thin, and steerable intravascular catheter is guided through the coronary vessel. At the distal tip of the catheter, a significantly minimized ultrasound transducer is mounted. The transducer generates high-frequency sound waves that reflect off tissue or vessel walls. The reflected sound waves are used to create a cross-sectional image (360-degree view) of the artery from within the vessel. Figure 1 shows a typical cross-sectional IVUS image of a diseased coronary artery.

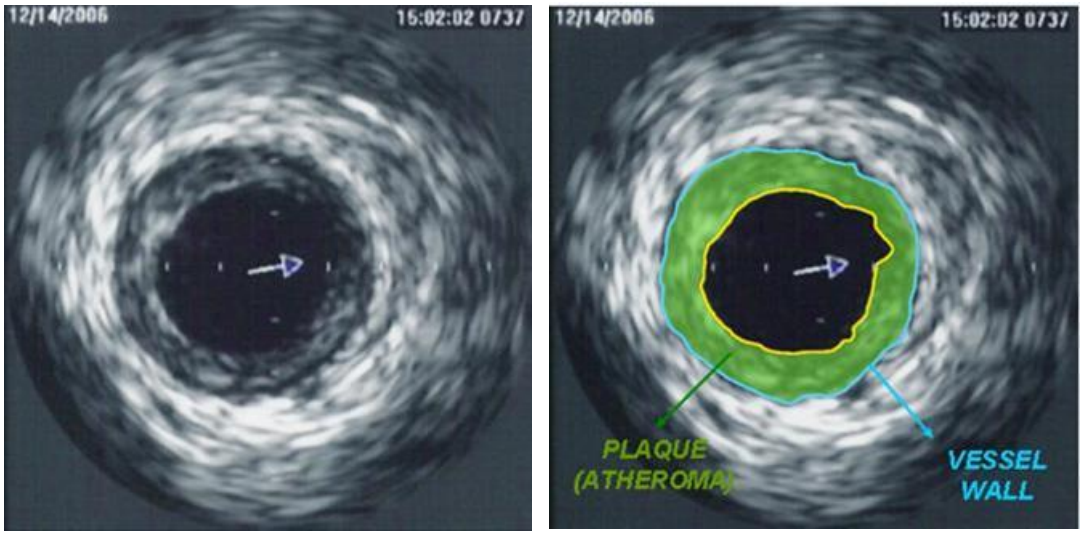


Figure 1. (Left) IVUS image of a partially occluded coronary artery. (Right) Color coding highlighting the lumen, the plaque and the vessel wall (adapted from [10])

Compared with X-ray angiography, which only displays a two-dimensional projection of the arterial opening, the penetrating nature of ultrasound enables detailed, high-resolution unique visualization of not merely the lumen but also the plaque "hidden" within the wall. IVUS precisely quantifies the extent of the plaque and provides detailed information about the shape and structure of the coronary vessels *in-vivo*. Another advantage of IVUS over angiography is that IVUS eliminates the need for introducing radio-contrast agents and therefore the patient is not exposed to any ionizing radiation.

Figure 2 shows a picture of a commercial IVUS system that includes a console for data processing and for reconstruction of images (Figure 2-left) and a catheter (Figure 2-right). Current commercial catheters are typically 2.5 to 3.5 French (0.87 to 1.17 mm) in diameter with lengths ranging from 90 cm to 150 cm.

Figure 2. Intravascular ultrasound (IVUS) system (The console of the Boston Scientific iLab®) with display (left) and the Atlantis™ SR Pro coronary imaging catheter (right) (Adapted from [9])

IVUS research started in the late 1980s. It was initially developed as a research tool but over time its clinical use increased and now IVUS has become an important

diagnostic supplement for percutaneous coronary intervention (PCI) in the treatment of coronary artery disease. PCI, which is commonly known as coronary angioplasty, refers to a variety of procedures used to treat the narrowed coronary arteries. Typically, PCI is performed to increase the size of the lumen by pushing the plaque deposits against the wall of the artery by a tiny balloon (balloon angioplasty). Balloon angioplasty may be accompanied with a stent placement to hold the artery open when the balloon is deflated and removed. During these therapeutic interventional procedures, IVUS is used as a visual guidance tool. Furthermore, after the PCI, there is a need to monitor the effects of the treatment techniques *in vivo* and the IVUS procedures are used to assess the clinical success of the therapies over time. Naming few examples, IVUS can be used to investigate the effects of lipid-lowering therapy or can be used to determine the need for re-stenosis based on whether the stent has been placed correctly or not. IVUS also helps the medical researchers by providing a better understanding on progression or regression of the plaque buildup [3].

One of the greatest challenges in the treatment of coronary artery disease is the early detection of the vulnerable plaques that are most likely to cause future adverse cardiovascular events such as myocardial infarction. Angiography does not easily distinguish vulnerable plaques from stable ones and every year thousands of deaths result from rupture of plaques that are deemed “insignificant” on angiographic evaluation. On the other hand, high-frequency ultrasound can be used to analyze the composition and morphology of the plaque. Therefore, IVUS is a more reliable tool compared to angiography at predicting the likelihood of a plaque rupture *in vivo*. In a recent study (Providing Regional Observations to Study Predictors of Events in the Coronary Tree -

PROSPECT) it was clinically demonstrated that IVUS can assess risk of a future event better than using angiography alone [11]. In another study the impact of IVUS guidance on long-term mortality after stenting of unprotected left main coronary artery is investigated [12]. The study showed that IVUS guidance reduces the 3-year mortality by 56% compared to angiography. Summaries of similar other studies that investigate the clinical advantages of IVUS guidance can be found in [13].

The IVUS systems are priced between $100,000 and $200,000 and the single use IVUS catheters cost up to $1000 each. The usage of IVUS has shown increasing growth in the past years and currently it is estimated that around 200,000 IVUS procedures are done every year in US [14]. Despite the increase in usage, the IVUS technology is still under penetrated worldwide primarily due to the lack of reimbursement for the procedure. It is estimated that IVUS usage within PCI procedures is 14% in the US and 4.5% in Europe [15]. On the other hand, in Japan, where IVUS imaging is reimbursed, majority of the PCI procedures (around 65%) utilizes IVUS as an aid. It is expected that the usage of IVUS will keep increasing over the years as the limitations of relying on angiography alone gets widely recognized.

1.2. Basic Principles of Ultrasound Imaging

1.2.1. Basics of Brightness-Mode Ultrasound Imaging

Figure 3 shows an illustration of a typical ultrasound transmit-receive cycle for a single transducer element. This operation of transmitting and receiving is referred as a pulse-echo operation. During the initial pulsing mode, the transmitter circuitry excites the transducer with a high-amplitude and short-duration electrical pulse. The transducer

converts the electrical pulses into acoustic pressure and generates ultrasound waves propagating at the speed of sound in a particular direction in the medium. Immediately following this transmit operation, the transducer element is switched to a receive mode and the receive cycle begins.

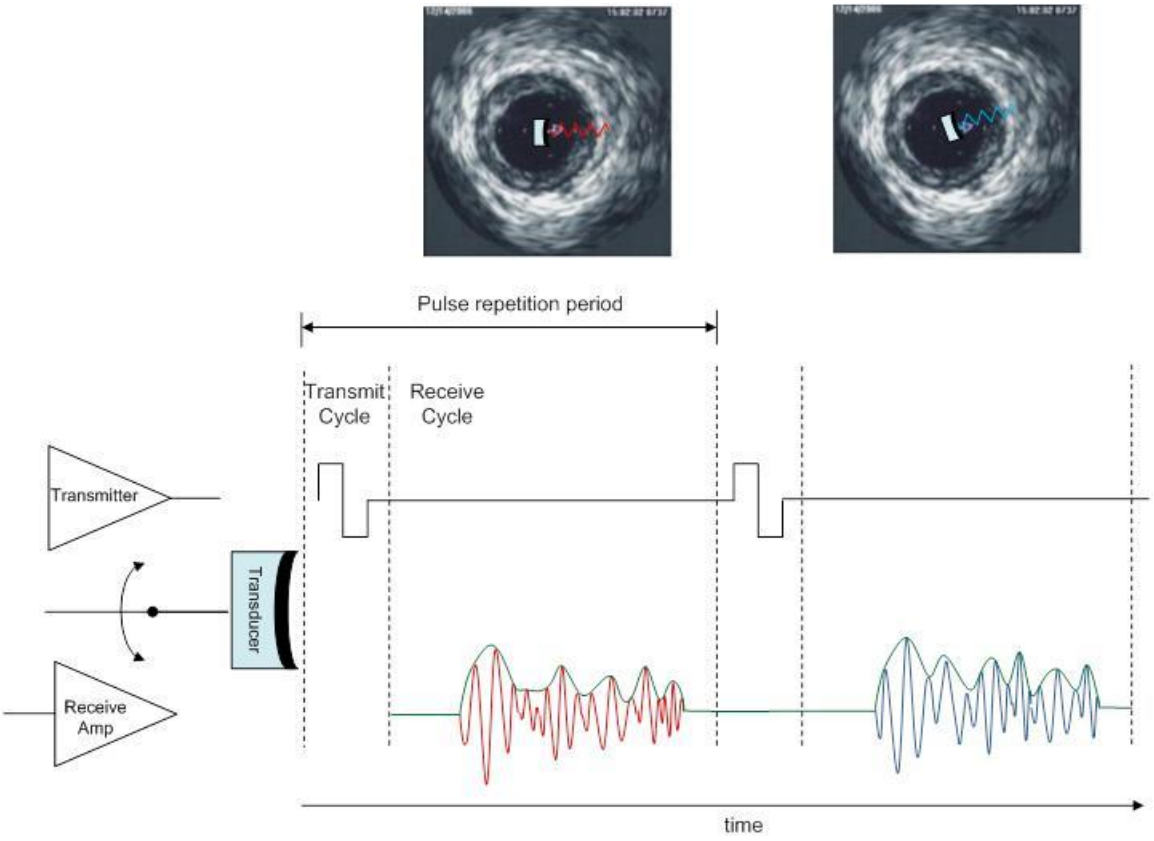


Figure 3. Illustration of the pulse-echo operation showing the transmit-receive cycle. After the ultrasound is generated in the medium in transmit cycle, the transducer connection switches to the receive amplifier. The receive cycle shows the A-scans generated by the transducer in response to the received echoes. The transmit-receive cycle is repeated until all the image lines are obtained to create the cross-sectional image.

The medium consists of layers of materials (i.e. tissue) with different acoustic impedances. The acoustic wave gets partially reflected back when it meets these layers with different acoustic impedances along the propagation path in the medium. The amount of the reflected acoustic wave is proportional to the difference of the acoustic

impedances. In other words, if the difference in the acoustic impedances is large, most of the incident ultrasound wave gets reflected. Similarly, if the difference of the acoustic impedances is small, which typically is the case at boundaries of soft tissues, a small percentage of the acoustic wave gets reflected, and most of the acoustic power continues propagating in the medium. The reflected wave, which is referred as an echo, travels back towards the face of the transducer. When the echoes reach and hit to the transducer element, the transducer converts the received acoustic pressure into electrical signals.

The distance of the reflector from the transducer can be found using the time difference between the initial transmitted pulse and the received echo. Assuming a constant speed for the acoustic wave propagation in the medium, the distance from the transducer to the reflector can be calculated using the following relationship:

$$D = \frac{ct}{2} \tag{1}$$

where D is the distance, t is the time of arrival and c is the speed of sound in the medium (nominally 1540 m/s for soft tissue).

The process to create images from the received echo responses is as follows. First, envelope (amplitude) detection is done on the received echo signals (Figure 3). Thus each transmit pulse and its echoes form an amplitude mode (A-mode) scan line in a particular direction. After each transmit-receive cycle, the transducer is rotated slightly and the transmit-receive cycle is repeated to acquire a new image line. Figure 3 illustrates the acquisition of two different image lines. This process is repeated until the complete scan of the two-dimensional cross-sectional image area is completed one scan line at a time. Thus, each cross-sectional image may contain information of hundreds of separate A-scans. To generate the greyscale cross-sectional IVUS images (shown in Figure 3-top)

from the acquired A-scans, the amplitudes of the received signals in each scan line are mapped to a brightness level where higher amplitude echoes are mapped as brighter in the image. Hence, these generated images are called brightness-mode (B-mode) images.

The duration of each transmit-receive cycle depends on the desired imaging depth because the system has to wait until the echoes from the deepest tissue come back. For instance, to construct an image with a depth of 1.5 cm, each receive period must be at least 20 μs. The pulse-repetition frequency along with the total number of the required scan lines determines the image frame rate. This indicates a tradeoff between the image frame rate and the imaging depth.

A volumetric image display is another ultrasonic imaging mode. In 3D imaging the received A-scans are rendered and presented on a volumetric image. Some images displayed in this mode are presented in Chapters 3 and 4.

Typically, a single transducer is used both as a transmitter and a receiver. However, it is also possible to use separate transducers dedicated for receiving and transmitting operations. This enables independent optimization of the transducers for their respective operation mode and it also removes the need of switching circuitry between transmit and receive modes. On the other hand, the trade-off is that this also requires two transducers for each pulse-echo operation which requires more area.

1.2.2. Lateral and Axial Resolution

The spatial resolution of an ultrasound system refers to the minimum separation between structures within the image that the ultrasound beam can distinguish. Spatial

resolution is commonly further sub-categorized into axial resolution and lateral resolution **(**Figure 4**)**.

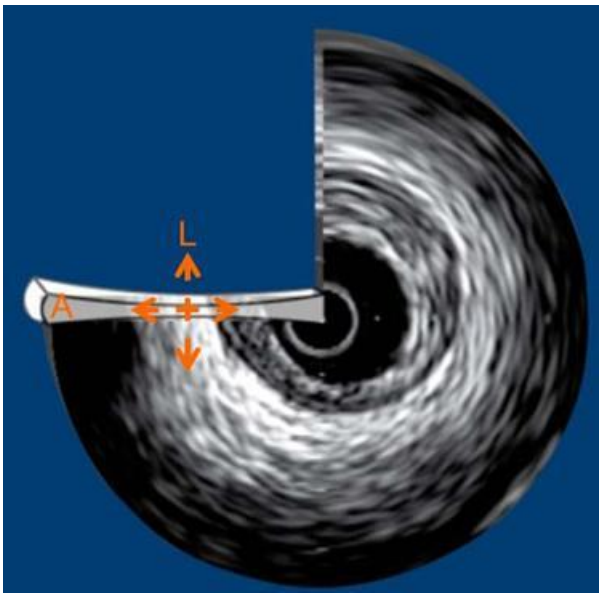


Figure 4. Illustration of the generated ultrasound beam showing the axial (A) and lateral (L) resolutions (adapted from [16])

Axial (also referred as azimuthal or longitudinal) resolution is the resolution in the direction along the axis parallel to the acoustic wave propagation.

$$Axial\ \mathrm{Re}solution = \frac{N\,x\,\lambda}{2} \tag{2}$$

where N is the number of cycles in the pulse and λ is the wavelength of the ultrasound signal corresponding to the frequency of the transmitted signal. Note that the transducer impulse response looks like a bandpass filter with a center frequency and a bandwidth. A higher bandwidth improves the axial resolution as it reduces the duration (# of cycles) of the transmitted ultrasound pulse and a higher bandwidth reduces the wavelength which also improves the axial resolution. One should note that the axial resolution does not

depend on the distance from the transducer (unlike the lateral resolution) and remains the same at any point in the scan line.

The lateral resolution is the resolution in a plane perpendicular to the direction of the ultrasound beam. The lateral resolution varies with the width (diameter) of the beam, and hence depends on the distance from the transducer (Figure 4). Along the beam axis there is an optimum point that is referred as the focal zone where the ultrasound beam has the smallest beam diameter providing the best lateral resolution. Away from the focal point (in the far field), ultrasound beams typically diverge, which decrease the lateral resolution. Similarly, at locations very close to the array, the beam is not focused, which also results in a decreased lateral resolution.

The axial length over which the beam remains relatively focused is referred as the depth of field. A typical measure of the depth of field is the distance over which the lateral resolution stays within the 3dB of the resolution at the focal point. The lateral resolution at the focal point is given with the below expression

$$Lateral\ Resolution = \lambda \times \frac{F}{D} \tag{3}$$

where F is the distance of the focal point from the transducer and D is the transducer diameter (aperture size). The ratio of the focal distance to the spatial dimension of the transducer (F/D term) is referred as the f-number. From (3), it becomes apparent that the lateral resolution at the focal point is directly proportional to the f-number and the wavelength. It should also be noted that the lateral resolution is generally few times poorer than the axial resolution.

1.3. Capacitive Micromachined Ultrasound Transducer

One of the most critical components of the ultrasound system is the transducer. Medical ultrasound imaging has been so far dominated by the piezoelectric transducer. High-frequency applications such as intravascular ultrasound imaging require transducer arrays with very small dimensions and extremely fine element spacing. However, piezoelectric transducers have severe bandwidth limitations and manufacturing difficulties for small sized arrays that prevent design of high bandwidth dense arrays with small dimensions. These limitations of the piezoelectric devices have impeded the improvement of the resolution of the IVUS images which would enable better visualization of thin fibrous cap and the vulnerable plaque. In addition, limitations of the piezoelectric devices also prevented the effective implementation of IVUS devices for emerging clinically important applications such as forward-viewing arrays for guiding interventions.

Capacitive micromachined ultrasonic transducer (CMUT), which has been developed during the past decade, had become a viable alternative to conventional piezoelectric transducer. CMUT has several manufacturing and performance advantages over piezoelectric transducers especially for IVUS [17, 18]. To begin with, manufacturing process for piezoelectric transducer arrays relies on labor-intensive steps and produces a low yield in small dimensions. This makes the manufacturing of piezoelectric transducer arrays for high-frequency IVUS costly and unpractical. On the other hand, silicon-based CMUT takes advantage of mature silicon microfabrication techniques and therefore enables cost-effective batch fabrication of very dense array structures with very small dimensions. Furthermore, microfabrication provides design

flexibility and allows fabrication of complex array structures such as highly populated 2-D arrays [19, 20] and ring annular arrays for forward-looking ultrasound imaging [21, 22]. Additionally, CMUTs are inherently non-resonant, broadband devices in liquid which improves the image resolution whereas piezoelectric transducers are resonant devices with limited bandwidth. Even with complex backing materials, which are used to improve their bandwidth, piezoelectric devices cannot achieve the resolution levels that CMUTs can provide [23]. Moreover, silicon micromachining technology makes CMUTs especially suitable for various levels of CMOS integration on a single substrate. On the other hand, piezoelectric transducers cannot be directly integrated with silicon integrated circuits. The electronics integration compatibility of CMUTs is a very critical advantage especially for IVUS application. This is because in IVUS applications the area is very limited and therefore compact integration with electronics is very critical for successful realization of IVUS arrays with smaller dimensions.

A commercial version of a CMUT-based 1.5D array was recently announced for mammary imaging [24]. This CMUT-based probe is not developed for a catheter application but it is worth noting here as it shows that CMUT technology is getting slowly adapted by the industry.

1.3.1. Principle of Operation

The basic CMUT structure consists of a top electrode buried in a suspended dielectric membrane, which is separated from a conductive substrate or a bottom electrode with a vacuum gap (Figure 5).

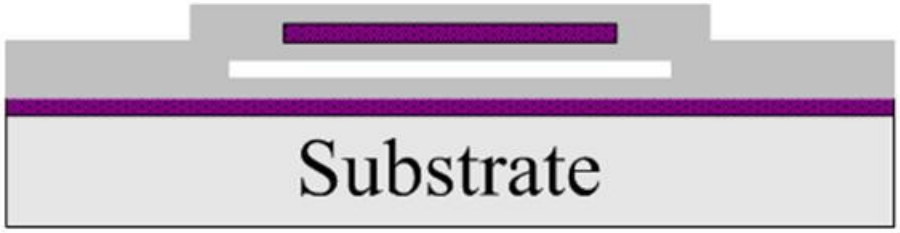


Figure 5. CMUT cross-sectional image.

A typical pulse-echo operation for CMUT is depicted in Figure 6. In this particular figure for clarity the transmitting and receiving CMUTs are separated but as mentioned earlier alternatively the same element can operate both as a receiver and a transmitter. During both transmit and receive modes, a dc bias is applied to one of the electrodes. During transmit mode, the membrane is driven with an AC pulse imposed on the bias voltage and ultrasound is generated in the medium through the vibration of the membrane. During receive mode, acoustic waves hitting the membrane cause the membrane to deflect which generates a detectable signal.

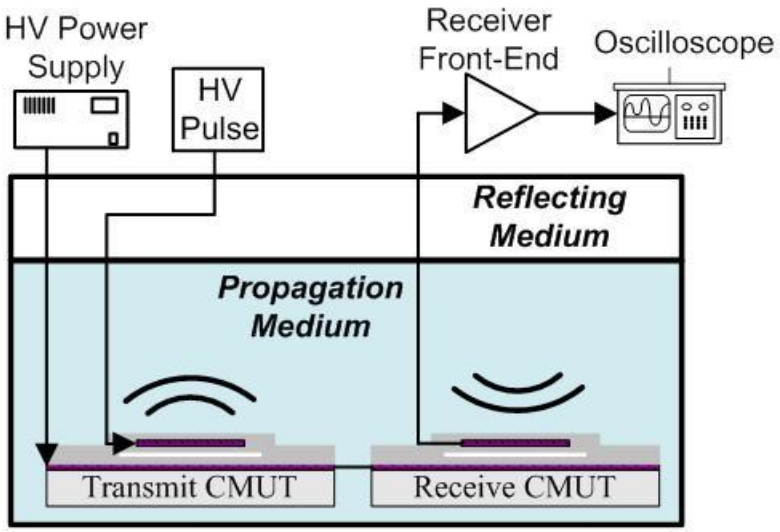


Figure 6. Pulse-echo operation with CMUTs

1.3.2. Electrical Equivalent Circuit

Using an electrical equivalent circuit is useful for first-order behavioral understanding of the CMUT and for modeling purposes of the transducer in circuit design simulations. The equivalent circuit model (Figure 7) presented here is based on Mason's model for parallel plate transducers [25]. In this model the membrane movement is assumed to be relatively much smaller compared to the vacuum gap, which is a well-suited assumption for modeling CMUT operation in the receive mode.

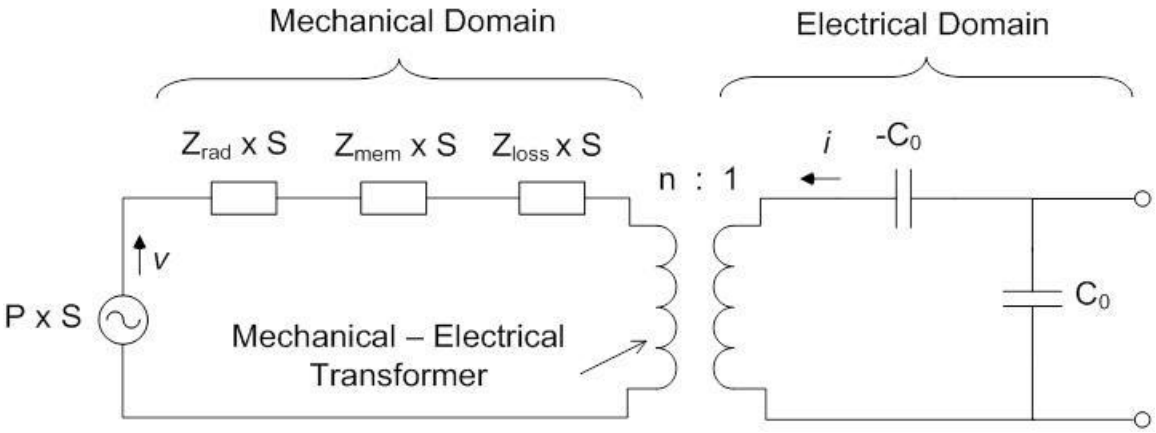


Figure 7. CMUT equivalent circuit

As seen in Figure 7, the equivalent circuit model is a two-port network, where the energy conversion between the electrical and mechanical domains is represented with a transformer. The mechanical domain and the electrical domain are on the two sides of the transformer. The average input pressure over the surface of the transducer is noted as P and S is the area of the electrodes. The force and velocity (v) in the mechanical domain are analogous to the voltage and current (i) in the electrical domain.

We will start discussing the components of the equivalent circuit by finding the expression for the transformer ratio first. Note that the motion of the CMUT membrane

due to the received ultrasound pressure modulates the sensor capacitance and generates a current signal that can be expressed as

$$I_{CMUT} = \frac{d}{dt}Q = \frac{d}{dt}\left(C(t)V(t)\right) = C(t)\frac{d}{dt}V(t) + V(t)\frac{d}{dt}C(t) \qquad (4)$$

Since the voltage bias of the CMUT is typically kept constant during the receive mode the first expression in (4) can be neglected. This implies that to find the CMUT current expression, as the next step, the time derivative of the CMUT capacitance term (*dC(t)/dt*) should be derived, which is discussed next.

Typically, in a CMUT, the bottom electrode is isolated from the vacuum gap with a layer of the membrane material (i.e. nitride) with a thickness noted as d_{is} in Figure 8. Similarly, the top electrode is also separated from the vacuum gap with a layer of membrane material with a thickness noted as d_{mem}. The thickness of the vacuum gap is noted as d_{vac}.

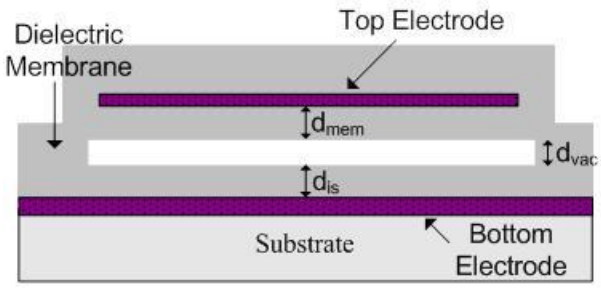


Figure 8. Cross section of a CMUT illustrating the thicknesses of the layers between the conducting plates.

The effective gap thickness, d_{eff}, between the two conducting electrodes with an effective relative permittivity equal to the vacuum permittivity can be given as

$$d_{eff} = d_{vac} + \frac{d_{is} + d_{mem}}{\varepsilon_r} \tag{5}$$

where ε_r is the relative dielectric constant of the membrane material. When the CMUT is biased with a DC voltage, the conducting plates are not exactly parallel to each other. However, an approximate value for the variable CMUT capacitance, C(x), can be found with a parallel plate approximation

$$C(x) = \frac{\varepsilon_0 S}{\left(d_{eff} - x\right)} = \frac{\varepsilon_0 S}{d_{eff}\left(1 - \frac{x}{d_{eff}}\right)} \approx \frac{\varepsilon_0 S}{d_{eff}}\left(1 + \frac{x}{d_{eff}}\right) \tag{6}$$

where ε_0 is the permittivity of free space and S is the area of the capacitor plates. Then the time derivative of the CMUT capacitance can be calculated using the derivative of CMUT capacitance in (6) with respect to displacement:

$$\frac{d}{dt}C(t) = \frac{d}{dx}C(x)\frac{dx}{dt} = \frac{C_0}{d_{eff}}\frac{dx}{dt} \tag{7}$$

In this expression, dx/dt is the velocity of the membrane, and the static bias CMUT capacitance (C_0) is given as,

$$C_0 = \frac{\varepsilon_0 S}{d_{eff}} \tag{8}$$

Using (7) in (4) the CMUT current can be written as

$$I_{CMUT} = V_{BIAS}\frac{C_0}{d_{eff}}\frac{dx}{dt} \tag{9}$$

where V_{BIAS} is the voltage applied to one of the CMUT electrodes that biases the device close to the collapse voltage. Note that the transformer ratio (n) converts the velocity (v) in the mechanical domain to a current (i) in the electrical domain and hence the CMUT

current expression can simply be expressed as the average membrane velocity times the transformer ratio:

$$i = n \times vel \tag{10}$$

Note that the unit of the transformer ratio (n) is expressed as A * s/m (or N/V). Finally, comparing the expressions (9) and (10), it becomes clear that

$$n = V_{BIAS} \frac{C_0}{d_{eff}} \tag{11}$$

In the electrical side of the equivalent model in Figure 7, the static capacitance of the parallel electrodes of the CMUT with applied DC bias is represented with a fixed capacitor (C_0). A negative imaginary capacitance ($-C_0$) is included to model the well-known spring softening effect [26].

The mechanical side of the model includes a term associated with the radiation impedance (Z_{rad}) of the membrane. Radiation impedance of the membrane is analogous to an electrical resistance and represents the ratio of the average pressure in the medium to the average velocity of the membrane. The radiation impedance is typically a complex quantity. However, when the transducer dimensions are relatively higher than the acoustic wavelength, the radiation impedance becomes mostly real [27, 28] and approaches to the acoustic impedance of the medium (R_{med}). Therefore, note that hereafter, in the equivalent circuit figures, Z_{rad} is replaced with R_{med}. As a numerical example, R_{med} is equal to 1.5 MRayls for water.

The mechanical impedance of the membrane is modeled with complex impedance, Z_{mem}. This membrane impedance can be represented with a series LC network which models the main resonant mode [26]. Z_{loss} represents the mechanical

losses in the membrane and can be replaced with a resistor in the model (Figure 9). Note that in the equivalent circuit model in Figure 9, the impedance related terms are scaled with S (the area of the electrode) since the mechanical input is given as Force (P x S).

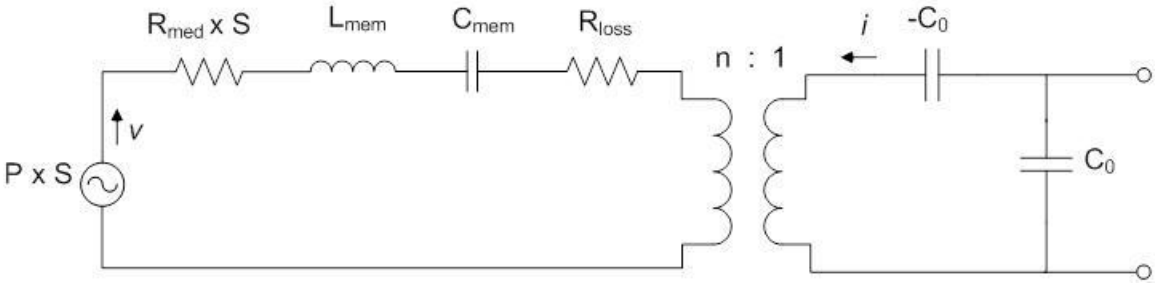


Figure 9. Equivalent circuit model for the CMUT element in receive mode. The membrane impedance is replaced with the LC circuit and the medium and loss impedances are represented with resistances.

The terms on the mechanical side can be referred to the electrical side using the transformer ratio (Figure 10). Typically the $C_{mem}\ x\ n^2$ term is much smaller than C_0, therefore the spring softening cap ($-C_0$) can also be neglected. In addition, the force term becomes a voltage term when it is reflected on the electrical side. The electrical port consists the input impedance of the receiving amplifier (Z_{amp}) and the parasitic capacitance between the CMUT and the receiver amplifier (C_{par}).

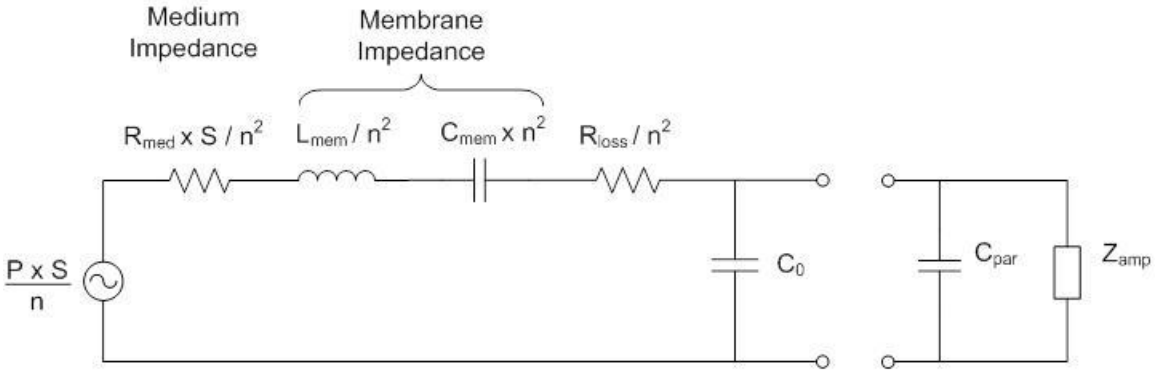


Figure 10. The circuit model where all the elements on the mechanical side are referred to the electrical domain. The electrical loading of the receive electronics is also shown.

For air applications, the impedance of air is almost negligible and the CMUT behavior is modeled with a resonant series RLC circuit containing the series membrane LC and the series R_{loss} term. On the other hand, when the CMUT is used in immersion (i.e. water, blood), which is the case for medical intravascular imaging; the mechanical impedance of the liquid dominates over the impedance of the membrane and the loss term. Therefore, the membrane and loss impedances can be neglected and the whole equivalent circuit can be simplified to a current source in parallel with the medium impedance and the CMUT capacitance (Figure 11). It should be noted that the loading of the liquid medium makes the CMUT inherently a non-resonant wideband device while operating in immersion.

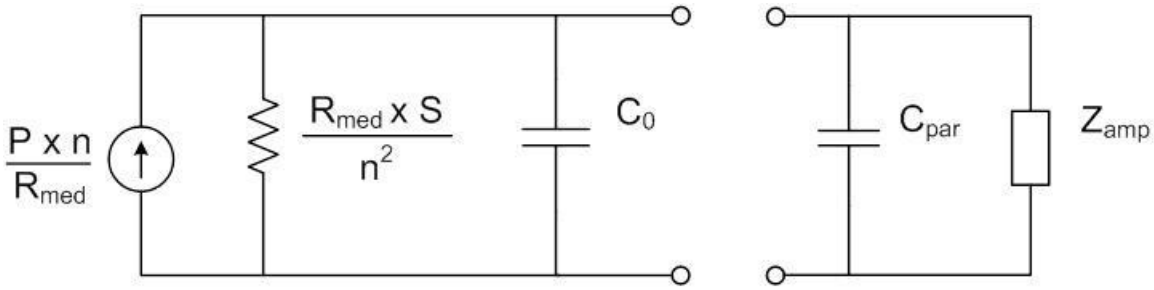


Figure 11. Simplified Norton equivalent circuit of CMUT in immersion along with the electrical loading of the receive electronics.

Note that, the medium impedance referred to the electrical side ($R_{med}S/n^2$) is for electrical modeling purposes and does not represent a physical resistance. Ideally, there won't be any dc current between the two electrodes of the CMUT. On the other hand, although being an insulator, the membrane material has some finite resistance resulting in a leakage current. For a practical CMUT, this leakage current is a very small value and can safely be neglected. Therefore, in circuit simulations, this equivalent circuit for

immersion operation should be connected to the receive amplifier over a decoupling capacitor to prevent a dc current flowing on the CMUT equivalent resistance.

The simple equivalent circuit that is briefly discussed in this section is accurate enough for first-order modeling of the CMUT for receiver electronics design. More detailed derivations of this equivalent circuit can be found in [26, 29]. An improved model [30] also incorporates the mechanical loading of the vacuum on the membrane impedance. A PSpice equivalent circuit based on this improved model is given in [31]. Also note that the model discussed here is not very accurate for transmit operation where the excitation voltages are large that invalidates the small-signal assumptions used in this model. Therefore, to accurately predict the behavior of the CMUT for large excitation voltages in transmit mode, a more detailed model should be used [31-34]. To get the most accurate results, finite element models that capture the full mechanical behavior of the CMUT can be used [35, 36].

1.4. High-Frequency Side-Looking IVUS

1.4.1. Motivation for High-Frequency Ultrasound

Better spatial resolutions can be obtained by increasing the operation frequency since both the lateral and the axial resolutions improve with a shorter wavelength. As a numerical example, at 10 MHz, a transducer with f#2.5 can have a lateral resolution of 375 μm. If the frequency is increased to 50 MHz, then the lateral resolution for the transducer with f#2.5 would improve to 75 μm [37]. Similarly, the axial resolution would also improve by 5 times. However, the improved spatial resolution comes at the expense of a reduced depth of penetration because the attenuation in the medium increases with

the increased frequency. As a result, high frequency ultrasound is more suitable for applications that do not require much penetration. For instance, a typical imaging depth for a 50 MHz system would be around 1 cm.

High-frequency ultrasound (above 30 MHz) is promising for many clinical applications that require superior resolution. Some of those clinical applications that benefit from high-frequency ultrasound imaging include eye (ophthalmology), skin (dermatology) and intravascular imaging of the coronary arteries [6, 38]. In ophthalmology, high frequency ultrasound is used for imaging of the anterior segments of the eye for diagnosis of ocular tumors and glaucoma [39]. In dermatology it is used as a non-invasive imaging tool to assess tumors [37]. High-frequency ultrasound imaging is currently also used in clinical research studies such as small animal imaging (i.e. mouse, rat) in evaluating diseases and drug and gene therapy [40].

1.4.2. Advantages of Phased-Array Systems

The ultrasound systems can be divided into two broad categories: systems using single element transducers and phased-array systems that utilize many transducer elements. Multi-element phased-array systems are desirable in medical ultrasound imaging applications because they offer few distinct advantages compared to the single-element transducer systems.

One of the biggest disadvantages of single-element systems is the fixed-focal point of the transducer, which significantly limits the depth of field. On the other hand, multi-element phased-array systems have many active channels that allows to steer the

ultrasound beams in any direction and to electronically focus the ultrasound energy at various desired depths [1].

In a multi-element array, the acoustic echo from the desired focal point reaches each receiving transducer element at different times because of the path length difference (Figure 12). Therefore, to focus to the desired point, signals received from each element should be properly delayed to compensate for this signal path length difference and to time-align the received acoustic signals as if they arrived simultaneously. This operation of adding the signals of each element after properly delaying them to implement focusing is referred as receive beamforming. Similar to the receive beamforming, in transmit beamforming, all array elements are excited with proper delays to produce a steered and focused acoustic beam where the sound waves converge on the desired focal point.

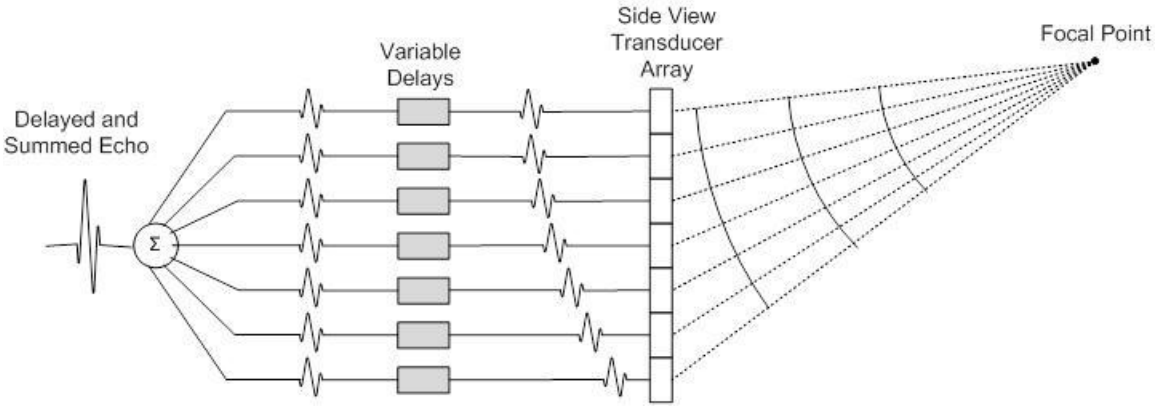


Figure 12. Simple block diagram of a receive beamforming system. The focusing operation requires implementation of specific delays for each channel.

Phased-array systems also enable a technique referred as dynamic receive beamforming. In dynamic receive focusing, the applied delays to the individual receive channels are adjusted dynamically to sweep the receive focal point along the scan line in real time. This enables to track the transmit pulse outward to maintain optimal focusing

over a much greater axial range and therefore resolution is enhanced for a greater depth (Figure 13).

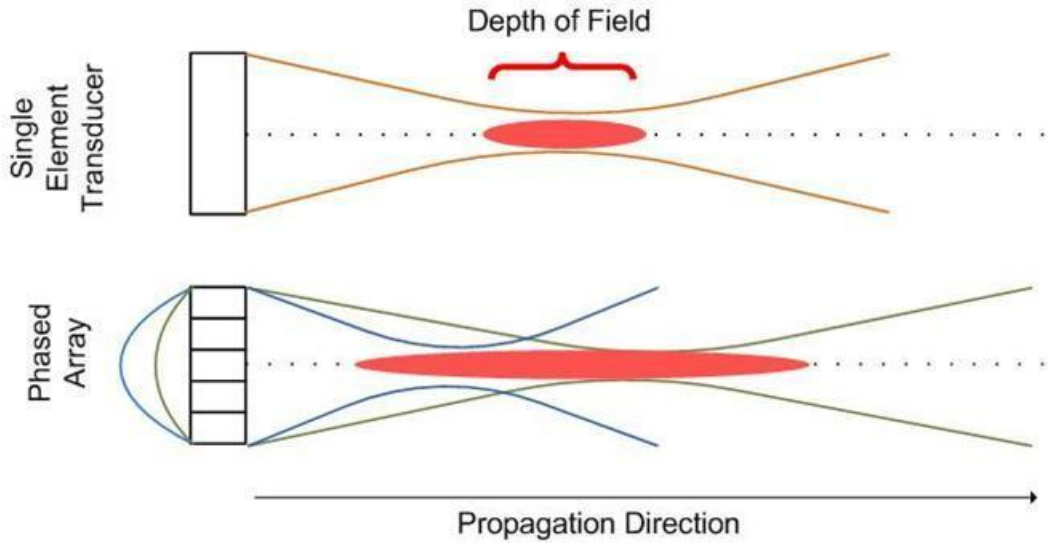


Figure 13. (Top) The wavefield (-3 dB contour) of a single element fixed-focus planar transducer. (Bottom) The wavefield of a multi-element phased array with dynamic focusing. In this figure the depth of field improvement of the phased array is demonstrated with two representative focal points.

In phased-array systems, the large number of active elements increases the cost of the system due to the need for dedicated receiver and transmitter circuits for each ultrasound element and makes it a big challenge to meet the size and power consumption requirements of the front-end system. In addition, the depth of field improvement of the phased-array systems using dynamic beamforming comes in the additional expense of increased complexity of the front-end system by the need to generate delays dedicated to each receive and transmit channel.

The required delays to steer and focus the ultrasound beam during transmit and receive can be accomplished through analog or digital techniques or a combination of both. In digital beamforming, the received signals are first digitized with an ADC and

then steering and focusing delays are introduced digitally. Digital beamforming concept has long been known but it was not feasible until the availability of high-speed ADCs. Currently, with the advances in digital electronics, digital beamforming is the dominant beamforming method in ultrasound systems. However in Chapter 6, it is discussed that for catheter-based applications analog beamforming approaches are more desirable considering the stringent power and interconnect requirements of the catheter systems.

1.4.3. Commercially Available IVUS Probes

It is worth reviewing the existing commercial catheters to discuss the challenges and current limitations for intravascular ultrasound imaging. There are many companies that provide ultrasound equipment (i.e. Sonosite, Philips, Siemens, GE, Honda Electronics, Teratech). However, for IVUS imaging currently there are only 3 dominant companies, which are Volcano, Boston Scientific and Terumo. Terumo is the market leader in Japan where Volcano and Boston Scientific lead the US market.

1.4.3.1. Rotational Systems

There are mainly two types of IVUS imaging systems currently in use. These are rotational/single element catheters and solid-state catheters. Both of these technologies create radial images of the vessels. The images are perpendicular to the probe, in other words they are side-viewing catheters, where the transducer array is mounted on the side of the probe.

In a rotational IVUS catheter, to obtain the cross-sectional image, a single piezoelectric crystal transducer located at the catheter tip is mechanically rotated at 1800

revolutions per minute by a flexible drive cable [41]. The single element transducer can be designed to operate at relatively high frequencies, thereby achieving a relatively high resolution. The commercial systems can operate at frequencies up to 45 MHz. A mechanically-scanned IVUS catheter with a single transducer element is illustrated in Figure 14-top. The single element system typically requires only two electrical connections. One of them is used to carry the transmit pulse and the other one is used to connect the transducer to the external receive amplifier. The transmitter, the receiver circuitry and the cables are stationary whereas the transducer element is rotating. Therefore, a rotary transformer is used to transfer the signal information between the rotating transducer and the stationary receiver and transmitter circuitry.

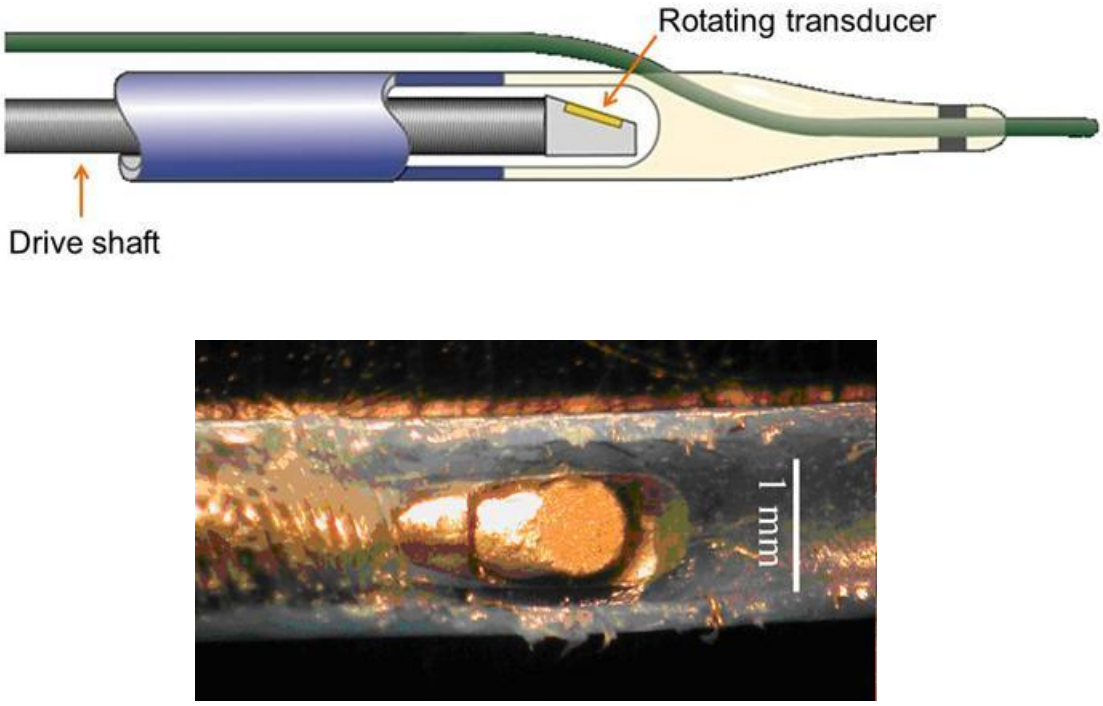


Figure 14. (Top) Illustration of the rotational side-looking IVUS system (image by Boston Scientific Corporation - obtained from [16]) (Bottom) Boston Scientific SoniCath 0.7-mm-diameter transducer secured in a test lumen [42]

The catheters are advanced in the vessels using a guidewire which is located outside the catheter running in parallel with the long axis of the catheter (Figure 14-top). Therefore, a guidewire artifact is seen in the image which prevents imaging of some of the tissue in the direction of the guidewire, so called the guidewire shadow. Another drawback of the rotating system is that the rotation of the transducer may not be even, which causes distortion in the image. This effect is known as NURD (non-uniform rotational distortion). In addition, during scanning the catheter tip may move relative to the vessel wall, which also results in image distortion.

1.4.3.2. Solid-State Systems

A more advanced type of IVUS probe employs a solid-state multi-element array catheter. The solid-state approach has the distinct advantage of having no moving parts within the catheter and therefore it does not suffer from the motion artifacts. Currently, commercially-available array-based catheter systems are offered by a single company (Volcano Therapeutics, Rancho Cordova, CA). In this solid-state approach, a 1D rectangular transducer array consisting up to 64 piezoelectric transducer elements with 20-MHz frequency is mounted cylindrically and wrapped around the circumference of the catheter body on the tip of the catheter (Figure 15).

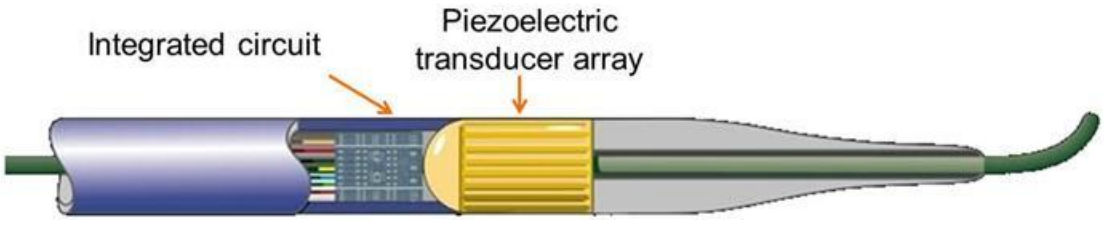


Figure 15. Schematic of the solid-state side-looking IVUS system (image by Boston Scientific Corporation - obtained from [16])

The system also incorporates a set of small custom-designed integrated circuits mounted on the tip of the catheter adjacent to the transducer array [43]. The details of the design of the chip that is very similar to the ones used in the commercial product are presented in [44]. Each chip is designed to interface with sixteen transducers and contains transmit circuits to generate 10-V pulses and 20-MHz current amplifiers to amplify the received echo signals. In transmit and in receive only a few of the array elements are activated at a time to reduce the required number of wires inside the catheter. To acquire the cross-sectional images, the activated transducer group is moved to adjacent transducers with the control of the electronic chips.

The sizes of the outer shaft of the 20-MHz commercial solid-state catheters are between 2.9 F (0.97 mm) and 3.5 F (1.17 mm) in diameter and the sheath size of the smallest version catheter is 5 F (1.67 mm). The details of the assembly of the piezoelectric array and the ICs in a solid-state catheter are explained in [45]. The construction of this probe is a labor-intensive task as it requires meticulous handcrafting to mount the whole system on a catheter. This increases the overall cost of the system combined with the costly transducer array manufacturing.

The existing solid-state array structure is suitable for dynamic focusing. However, this would require implementation of complex receive and transmit beamforming circuitry, which was not integrated on this catheter-based probe because of the size and power constraints. Therefore, this multi-element transducer system does not take advantage of the conventional phased-array operation and beamforming is limited to synthetic data acquisition techniques, which produces poor image SNR [46]. To improve

the SNR, the system requires averaging over multiple acquisitions, which reduces the frame rate.

1.4.4. Types of Transducer Arrays for SL-IVUS

In addition to the commercially-available cylindrical solid-state array, a wide variety of other transducer array configurations are currently in development for catheter-based ultrasound applications. In this section some of the alternative array types are reviewed. Some of these possible array configurations for side-looking catheter applications are illustrated in Figure 16.

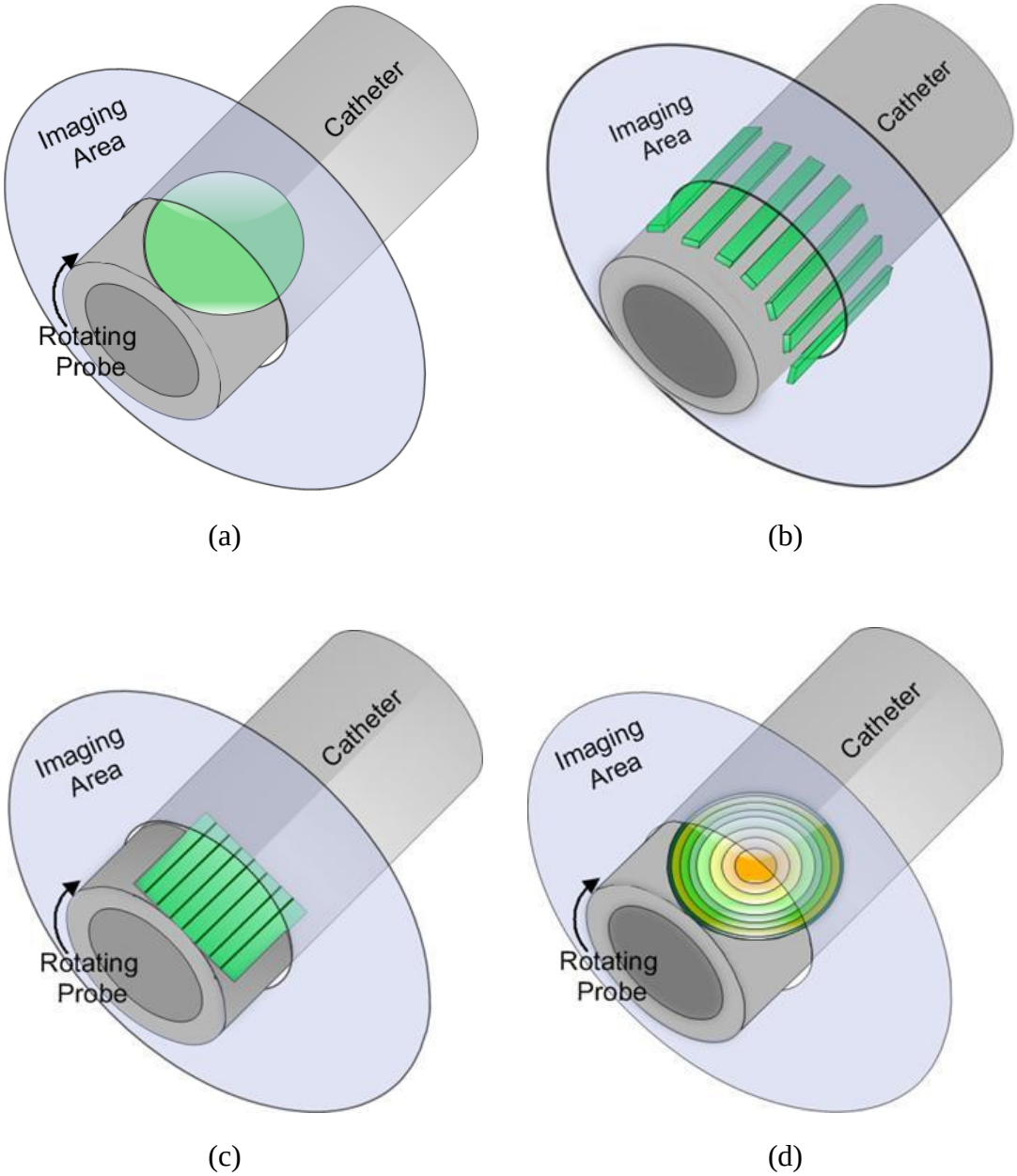


Figure 16. Examples of side-looking catheter probes. (a) Rotating single transducer (b) Cylindrical solid state array (c) Electronically scanned 1D phased array (d) Rotating phased annular array

1.4.4.1. 1D Phased Arrays

A 1D array (also referred as a linear array) is the most commonly used transducer array in the ultrasound medical imaging. A 1D array contains an array of long and thin transducers (Figure 16) and the number of elements in a typical 1D phased array ranges from 32 to 128. A discussion of a commercially-available 64-element side-viewing 1D phased array developed for intracardiac echocardiography (ICE) imaging can be seen in [47]. A 1D array allows electronic focusing and steering in the azimuth (lateral) direction, however, in elevation there is only a single focal point, which is typically provided by a lens. Therefore, the image quality is significantly degraded in the elevation direction. In a 1D array, typically, the resolution in elevation is 3 to 5 times worse than the resolution in the azimuth direction.

1.4.4.2. 1.5D Arrays

Poor focus of 1D array in elevation can be addressed by using multi-row arrays such as a 1.5D array, which is an intermediate between 1D and 2D arrays. In 1.5D arrays elevation aperture is divided into few sub elements [48, 49]. Each sub element is delayed dynamically to focus in the elevation direction with phased electronics. This provides an improved resolution in the elevation direction over an extended scan range.

1.4.4.3. 2D Rectangular Arrays

In a 1.5D array the beam steering is restricted to the azimuth dimension and the focusing in elevation is still worse than the focusing in the azimuth direction. In 2D arrays the elevation focusing is improved by finely dividing the transducer array also in

the elevation direction. This allows electronic steering and focusing of the beam in both directions and enables to image the entire volume. In a 2D array, the number of elements in the elevation direction is typically the same as the number of elements in the azimuth direction.

It should be noted that 2D arrays provide the best image quality. On the other hand, on top of the piezoelectric manufacturing issues [50], 2D arrays also have the maximum complexity due to the large number of transducer elements and the sheer complexity of the front-end circuitry. So far, the complexity of 2D arrays did not allow successful implementation of 2D array based systems. Some studies tried to address the interconnect complexity of the 2D array systems. For instance, integration of the beamforming circuitry and multiplexing on the probe close to a 2D array to reduce the number of interconnects is employed in [51]. In [19], a CMUT based 2D array system with a time-domain multiplexing method is proposed to address the interconnect problem. A 2D phased-array system based on CMUTs tightly coupled with front-end electronics is shown in [52]. For catheter-based applications in particular, progress in the implementation of 2D arrays based on piezoelectric transducers are reported in [53] for side-looking intracardiac echocardiography (ICE) and for forward-looking IVUS imaging [50].

1.4.4.4. Annular Arrays

Annular arrays contain transducer elements in a configuration of concentric annuli (Figure 17). They are axially symmetric and therefore can produce high quality narrow, axisymmetric beams [54]. In addition, they maintain identical beamwidths throughout the

entire imaging depth in both lateral direction and the elevation direction thanks to the circular aperture (radial symmetry). On the other hand, an annular array cannot generate volumetric images because it is not able to provide beam steering and the focusing is limited on its axial line.

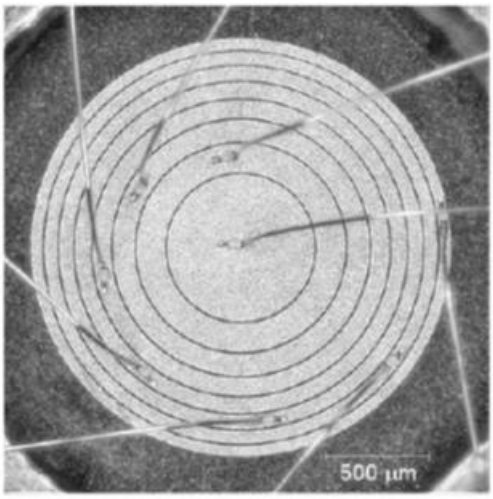


Figure 17. 2-mm diameter 8-element piezoelectric annular array [55]

The 2-way PSFs of different structures (single circular transducer, solid-state 1D array and phased annular array) are simulated and compared in [56]. PSF simulation results showed that the annular array produces the best beam patterns compared to the other configurations. In addition, compared to a 1D array, an annular array has less number of elements with larger area yielding improved SNR. Another advantage of annular arrays is that the reduced number of channels enables practical implementation of the receiver and beamforming electronics within the probe. Because of these various advantages, annular array is the choice for the implementation of the side-looking IVUS probe, which is discussed in the next section.

1.4.5. IVUS Probe Using Annular CMUT Arrays

Although phased arrays are desirable for improved image quality, all of the commercially available high-frequency (above 30 MHz) IVUS systems are based on a single element transducer, which as discussed earlier has a fixed focal distance suffering from a limited depth of field [38, 39]. Recently in 2008, a high-frequency system based on an ultrasound array has become commercially available (Vevo 2100, Visualsonics Inc., Toronto, Canada). This system is based on a linear array with 256 elements equally spaced at 38 μm [57] with center frequencies ranging from 15 to 70 MHz and can provide a resolution as low as 30 μm [58]. However, it should be noted that this system is mainly used for small animal imaging and is not targeted for IVUS. The only commercially available array system targeted for IVUS application is the side-looking solid-state system discussed in section 1.4.3.2, which is limited to ultrasound frequencies up to 20 MHz (well below the 45 MHz systems based on single element transducers).

Several researchers have reported the development of high-frequency annular arrays based on piezoelectric transducers [54, 55, 59-64]. However, the smallest piezoelectric annular arrays demonstrated so far have diameters on the order of 2 mm. The previously-mentioned manufacturing difficulties of piezoelectric transducer arrays for high-frequency operation have been a major limitation in the realization of high frequency ultrasound array systems with smaller diameters. On the other hand, CMUTs are well suited for high-frequency ultrasound applications [65]. A CMUT based annular array design is reported in [66], however, the target use of this design is RF ablation therapeutic ultrasound. The designed CMUT array has an operation frequency of 2.5 MHz and the diameter is 3 cm, which is very large for use in IVUS imaging.

Figure 18-left shows the micrograph of an actual CMUT annular array designed and fabricated for catheter-based IVUS imaging application. The target catheter diameter size is 1 mm and hence the annular array is designed with a 0.84 mm diameter. Annulus has 21 ring shaped, 18 µm wide, 60 µm long curved CMUT membranes separated by 2 µm. The rings are connected to each other to form 8 similar-area transducer elements as shown in different shades of gray Figure 18-right. Further details of the fabrication and design of this CMUT annular array can be found in [56, 67]. A conceptual diagram of a SL-IVUS imaging system employing this high-frequency CMUT annular array with integrated electronics mounted on the side of the catheter is shown in Figure 19.

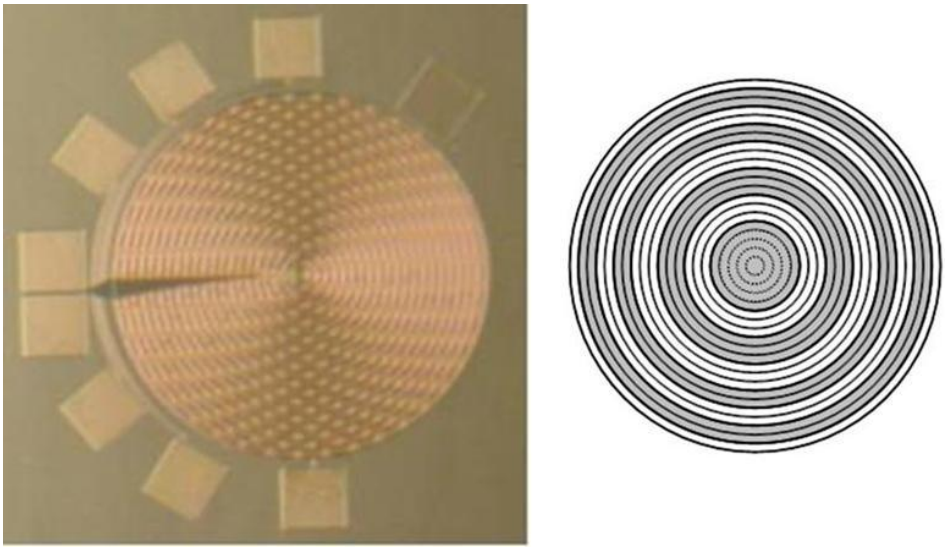


Figure 18. The micrograph of an 8-element CMUT annular array with 840-µm diameter and operating over 20-50 MHz band. The illustration on the right shows the 8 elements separated with different shades of gray.

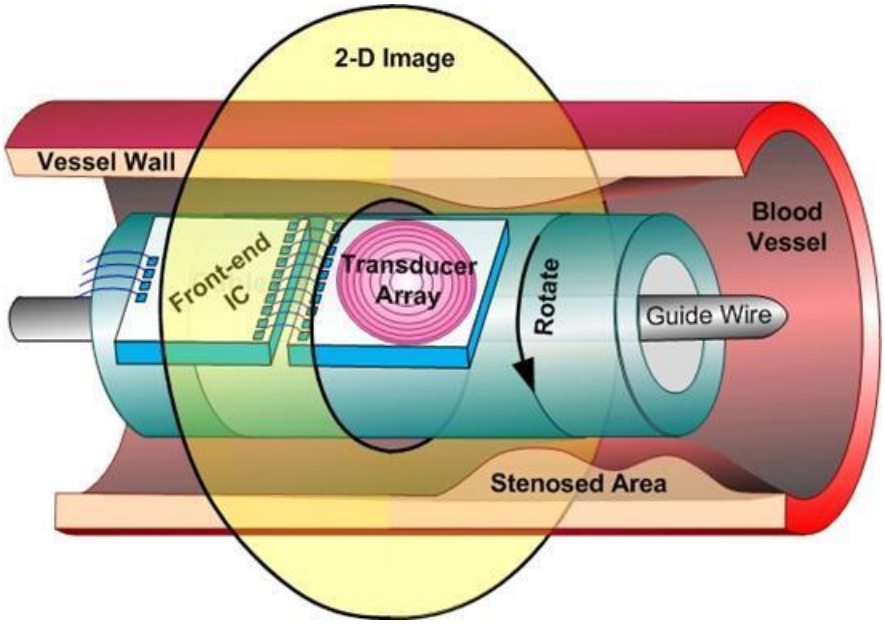


Figure 19. A conceptual diagram of a SL-IVUS probe employing an annular array integrated with electronics. Preamplifiers and the beamforming circuitry are integrated with the transducer array inside the catheter. The catheter is rotated and pulled back to form cross-sectional images of the vessel opening and the vessel wall.

The bandwidth of the current solid-state SL-IVUS probes with cylindrical array transducers is limited to 20-30% around 20 MHz operation frequency, which yields around 60-µm axial resolution [6]. For the commercially available 40-MHz single-element IVUS transducers the typical resolution is around 200 µm laterally and 80 µm axially [16]. This constitutes an important limitation for detection of vulnerable plaques which require axial resolutions as low as 30 µm [38]. In comparison, the high-frequency CMUT arrays can provide much better resolutions. For instance, the experimental results in [56] showed that, the measured 6 dB fractional bandwidth of the CMUT annular array element (shown in Figure 18) is 40% around 50 MHz. The measured lateral resolution (6-dB main-lobe beamwidth) is 120 µm and the theoretical axial resolution of this array is around 20 µm. This 20-µm theoretical axial resolution of the CMUT annular array is a significant improvement over the existing solid-state and single-element IVUS catheters,

and should enable high resolution imaging of cap thickness of plaques, which is critical for early diagnosis of vulnerable plaques.

1.5. Forward-Looking Volumetric IVUS Imaging System

Current commercially available IVUS systems only offer side-looking capabilities forming cross-sectional images of the vessel wall and cannot generate images of the volume in front of the catheter. To image a plaque, the side-looking catheter needs to pass through the lesion first which makes it unusable for chronic total occlusions (CTOs) where the blood vessels are totally occluded. CTOs are encountered in approximately 30% of all diagnostic coronary angiograms [68]. Without a forward looking capability, continually maintaining the guidewire within the limits of the vessel to avoid coronary perforations is a formidable challenge. Therefore, due to the limitations of current side-looking IVUS systems, it is very difficult to deal with CTOs in coronary arteries where the success rate averages around 50% [68]. Consequently, revascularization of the CTOs are attempted on only a minority (10%) of the total interventional procedures [69].

Forward-looking (FL) IVUS is an emerging, clinically important imaging modality, which enables to obtain images of the volume in front of the catheter. Such a forward-viewing device would be very useful for dealing with CTOs in the blood vessels for many reasons [69]. First of all, during CTO interventions, forward-viewing capability provides directional information for the therapy as it enables to see the position of the guide wire with respect to the vessel wall. This can significantly improve the procedural success rate of CTO crossings [70]. In addition, a FL-IVUS catheter incorporated with IVUS-based techniques such as virtual histology can provide information about the

composition of the CTO without first crossing it [71]. This is important because knowing the morphology and topography (i.e. the length of the occlusion) features of CTO ahead of time is useful in evaluating the risk of the crossing procedure. This may help in selection of the proper interventional therapy of nearly or totally blocked arteries [72]. For instance CTO operations are less successful when the CTO is older containing more calcified tissue.

There are several other potential advantages of a forward-viewing IVUS catheter. For instance, in side-looking IVUS systems, the blood flow is perpendicular to the image plane prohibiting the use of Doppler based flow measurement. On the other hand, FL-IVUS can be used for Doppler ultrasound processing since the flow direction is parallel to the ultrasound beam. Furthermore, FL-IVUS can help visually guiding stent placements, and monitoring ablation operations in the heart.

Although it has many potential clinical advantages, a FL-IVUS system is not commercially available yet. The initial efforts for forward-looking imaging were based on mechanical motion of a single piezoelectric transducer to generate 2D forward viewing planes [72] or 3D volume images [73]. However, these systems are costly and not practical due to their need for complex mechanical rotation systems. Another mechanically-scanned single-element based forward-looking IVUS probe is currently under development by Volcano Corporation (Rancho Cordova, CA, USA) and is undergoing preclinical evaluation. Figure 20 shows an illustration of this probe where a single 45-MHz piezoelectric transducer tilted at a 45^{o} angle at the tip of the catheter rotates to provide a forward-looking cone of visualization [9, 68]. The CTO completely blocking the artery is also illustrated in the figure.

This approach needed to use a single-element transducer instead of an array mainly because for a FL-IVUS application the required catheter tip diameter is very small (~2 mm), which challenge efforts to mount a transducer array at the tip of the catheter using existing piezoelectric technology. One of the drawbacks of using a single transducer in this application is that the acquired image is a cone and not a true volumetric image. In addition, the catheter needs to be mechanically rotated, which brings a risk of creating imaging artifacts associated with the rotational systems.

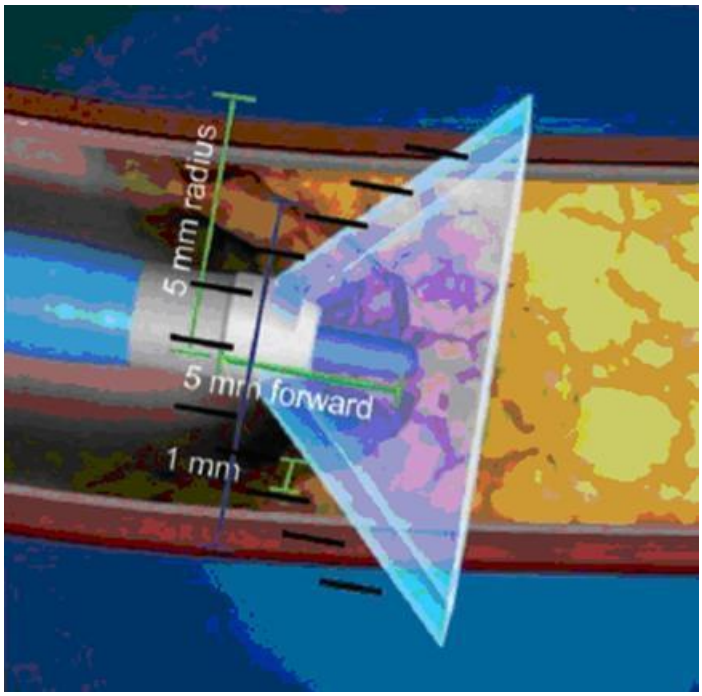


Figure 20. Illustration of a forward-looking IVUS catheter in development by Volcano Corp., Rancho Cordova, CA, USA [9].

In [74], a high frequency FL-IVUS system was proposed where a 64-element side-looking piezoelectric transducer array was modified to add a forward-looking imaging capability. The 1D array was arranged around a 1.2-mm diameter ring configuration. However, numerous missing elements of the prototype prevented to obtain

clinically-acceptable forward-viewing images. The works in [75, 76] also investigated the implementation of a forward-viewing ring array using piezoelectric transducers; however the resulting arrays had a poor yield, limited center frequency and bandwidth. In summary, it can be stated that so far the fabrication limitations of piezoelectric transducer technology for small dimension arrays have prevented effective implementation of practical forward-looking systems with diameters below 1.2 mm.

The latest developments in CMUT technology enable the microfabrication of capacitive transducer arrays suitable for catheter-based FL-IVUS application. Some recent studies demonstrated the feasibility of CMUT-based donut-shaped ring arrays for FL- IVUS [21, 22, 77, 78]. Typically, a full disk transducer array would provide a better image quality. However, the need for a guidewire in the center prevents the use of full aperture and motivates a ring array. The central opening can also be utilized for other therapeutic tools during interventions such as RF ablation or for photo-acoustic imaging. A ring-array is preferred over a 2D-array structure for FL-IVUS because a ring array can provide volumetric images without the complexity of a 2D array.

Recently, an approach with separated rings for transmit and receive operations is introduced by the Degertekin group [78]. Separating transmit and receive rings enables separate optimization of the transducer design and separate biasing for transmit and receive operations. Figure 21–left shows a picture a dual-ring CMUT array capable of volumetric imaging and suitable for fitting onto the front-tip of the catheter. Figure 21-right is an illustration of a FL-IVUS probe implemented using a CMUT array integrated with front-end receiver electronics. One should note that this CMUT-based system uses a

solid-state approach for volumetric imaging and doesn't require any rotating parts in the catheter.

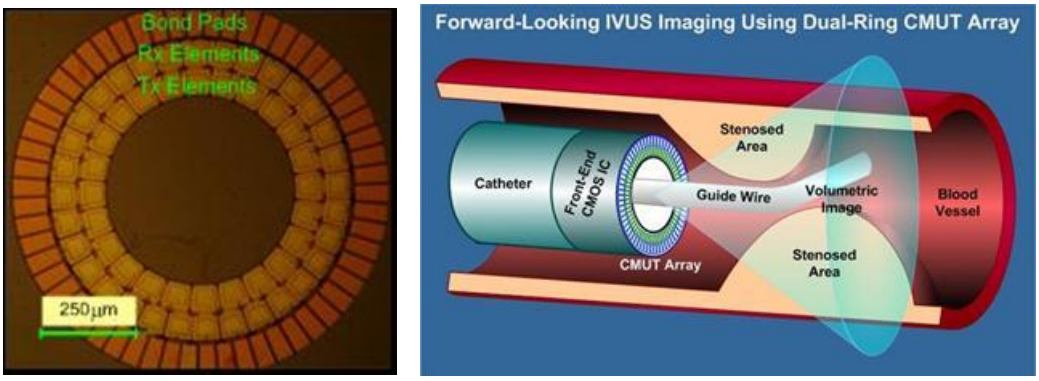


Figure 21. (Left) Dual-ring CMUT array; (right) forward looking IVUS probe with dual ring CMUT array

1.6. Motivation for Close Integration of Electronics for IVUS

The ability to integrate electronics is a key factor for successful implementation of catheter-based imaging arrays such as ring annular arrays [21, 22] and densely-populated 2D arrays [19, 20] for several reasons. First of all, for catheter-based applications, such as side-looking and forward-looking IVUS, the maximum number of interconnection cables is limited by the catheter diameter. Similarly, for a 2D array, having a dedicated cable for each transducer element is not practical as it would require excessive number of cables. Electronics integration close to the transducer array enables to reduce the required number of cables by implementing multiplexing. Furthermore, the signal levels are limited for small transducer elements in a 2D array or a ring array for a catheter application. In addition, for forward-looking IVUS imaging, conventional phased-array operation is not utilized since it would require prolonged data acquisition times, which would introduce significant image artifacts. Instead, synthetic aperture data acquisition

where a single element pulses and a single element receives, is used. In addition to the small transducer size, this synthetic data acquisition further limits the available signal levels. Therefore, efficiently handling the available signal levels and minimizing the receiver electronics noise level is very critical to achieve the required SNR levels. In the following paragraphs it is discussed that, especially for small transducers with large impedances, closely integrating the electronics with the transducer has a significant SNR advantage compared to a cable connection.

Typically, in ultrasound systems the transducer elements are connected to the electronics front-end through coaxial cables. For many ultrasound systems, the input impedance of the amplifier terminating the cable is designed to be 50 Ω to match to the cable impedance. In that case, the voltage generated by the transducer gets attenuated depending on the ratio of the 50-Ω termination resistance and the impedance of the transducer. Typically, for large transducers with small impedances, this does not introduce significant signal loss. As a numerical example, the impedance of the transducers in [60] is noted as 70 Ω – j200 Ω. Note that in that study the used circular transducers are quite large with a 1.3-mm radius. Terminating this large transducer, which has a small impedance value, with a 50-Ω amplifier does not degrade the signal at the amplifier input significantly. Therefore, matching the impedance of the amplifier to the impedance of the connected cable (or to the transducer impedance in a directly connected system) becomes the primary amplifier design target for interfacing with large transducer elements.

On the other hand, now consider a small transducer with an impedance value on the order of 100 kΩ, which is a typical value for tiny transducer elements for catheter-

based arrays or 2D arrays. In that case, even neglecting the losses in the cable, the voltage signal generated by the transducer gets attenuated by a factor of 2000 at the 50-Ω amplifier input. If the transducer would instead be terminated with a 100-kΩ impedance, the detected voltage signal would be increased by 60 dB. This clearly indicates that terminating the high impedance transducers with a high-impedance amplifier is strongly desired to improve the SNR. However, terminating a cable using a high-input-impedance preamplifier in a high frequency system results in undesired standing waves in the cable [79]. Therefore, to be able to realize a high-input-impedance preamplifier, the amplifier should be placed before the cable.

In addition to improving the sensed signal levels, the close electronics integration eliminates the parasitic interconnect capacitance of the cable connection, which could easily overwhelm the transducer capacitance and hence increase the system noise. Furthermore, the closely coupled electronics helps in miniaturization of catheter probes, eases the packaging requirements and thus reduces the system cost.

For the side-looking IVUS application discussed in section 1.4.5, another advantage of close electronics integration is that it enables to integrate the beamforming electronics in the probe. Typical ultrasound systems have one coaxial cable connecting each transducer element to its respective electronics. However, for this catheter-based application where the probe is rotated for image acquisition it is critical to minimize the number of interconnection cables. This can be achieved by integrating the beamforming circuitry with the transducer array inside the catheter on the ultrasound probe handle. After beamforming is achieved internally, only a single coaxial cable is required to transfer the data for the entire array to the external signal processing rather than a

dedicated one for each array element. In addition, beamforming on the catheter eliminates the need for power-consuming multiple high-speed output drivers.

1.7. System Level Considerations

Several system level issues should be taken into account for a successful implementation of a complete catheter design. Catheter-based ultrasound imaging is one of the many biomedical applications where one of the main considerations is the electrical safety. During the operation of the CMUT based IVUS catheters, it might be necessary to have internal dc bias voltages on the order of 100 V and pulse amplitudes up to 40 V. In the event of high-voltage or current surges the catheter must be electrically safe. Any breached dielectric insulation in the catheter presents a risk of exposing these high potentials to the patient or to the operator.

There are certain standards that regulate ultrasound catheter devices set by organizations like the Food and Drug Administration (FDA) in the USA. As an example, currently, IEC_60601-1 is one of those standards that regulate the electrical safety requirements for medical equipment. To get this safety approval the final catheters should pass high-potential and leakage-current tests. In high-potential testing, the outer shaft of the catheter is electrically stressed at high voltages for prolonged durations to evaluate the insulation against voltage leaks and the breakdown voltage of the outer shaft. As an example, in [80] it is noted that the catheter must "dielectrically withstand 3,000 volts for 60 seconds between the external surface of the catheter and any internal conductors or electrically active components when internal voltages are greater than 50 volts." Similarly, for leakage-current testing, in [80] it is noted that "any leakage current must be

less than 50 μA when 264 V is applied to the internal conductors." The results of these tests for a commercial side-looking ICE catheter (Siemens AcuNav™) can be seen in [81]. One should note that it is vital and challenging to implement materials with very high dielectric strength that would retain dielectric breakdown protection with the little volume dedicated for insulation material within the catheter.

The excitation pulse voltage should be as high as possible to obtain the best SNR. However, the total transmitted acoustic power cannot be arbitrarily high because the maximum power that can be transmitted within the patient is also strictly regulated and limited by the FDA. Exceeding the safe doses for the patient increases the relative risk of adverse mechanical events such as excess heating of the tissue and cavitation. One of the metrics that is used to characterize the safe limits is the spatial peak-temporal average intensity (I-SPTA), which is the maximum intensity occurring in an ultrasound beam averaged over the pulse repetition period [82]. For intravascular ultrasound this limitation is set as 430 mW/cm^2 [14, 83]. Another metric is the mechanical index (MI), which is an estimate of the maximum amplitude of the pressure pulse in tissue [84]. As an example, I-SPTA and MI values of a commercial catheter can be seen in [85].

Another concern regarding the power dissipation is the overheating of the ultrasound probe. In particular for IVUS application, the probe is located inside the human body therefore over heating can be a serious problem. Especially, for catheter systems that have many array elements packed in a very small volume, the self-heating of many transducers, the power dissipation of the phased array operation and the front-end electronics may introduce excessive heat. The heat should be transferred and dissipated from the catheter to keep the temperature rise within the safe limits in the catheter interior

and the surrounding tissue. In [86], 65 mW is given as the upper limit considering the temperature increase of both in air and in liquid conditions. The particular probe that is considered in that study contains a 1D array with a size of 2.6 mm in elevation and 6.4 mm in length. For smaller size arrays the power limitation might be smaller. To come up with a precise prediction of the power consumption limits, thermal dissipation models of the probe can be developed [86, 87]. It should be noted that, it is harder to dissipate power in air since cooling is much weaker and therefore temperature rise is more pronounced when the device is operated in air.

In [66] it is mentioned that CMUTs are advantageous compared to piezoelectric devices in regards of self-heating because CMUTs have less dielectric losses and a higher thermal conductivity. The work in [87] compares thermal efficiency of CMUT and PZT probes and verifies the thermal dissipation advantages of CMUT.

In addition to the electrical safety and the acoustic power limitation, there are many other standards in effect imposed by FDA for final market approval of the devices. Some of the other standards that the catheter needs to conform are in the areas of biocompatibility, packaging, sterilization and mechanical safety. Again, as an example, a recent FDA approval document for one of the commercial catheters on the market can be seen in [88].

CHAPTER 2

INTEGRATED FRONT-END ELECTRONICS FOR CMUT INTERFACING

In ultrasound imaging, the front-end electronics components are as important as the transducer in determining the overall system performance. A typical ultrasound front-end system mainly includes a receiver chain, a high-voltage transmitter and a transmit-receive switch dedicated to each transducer element (Figure 22).

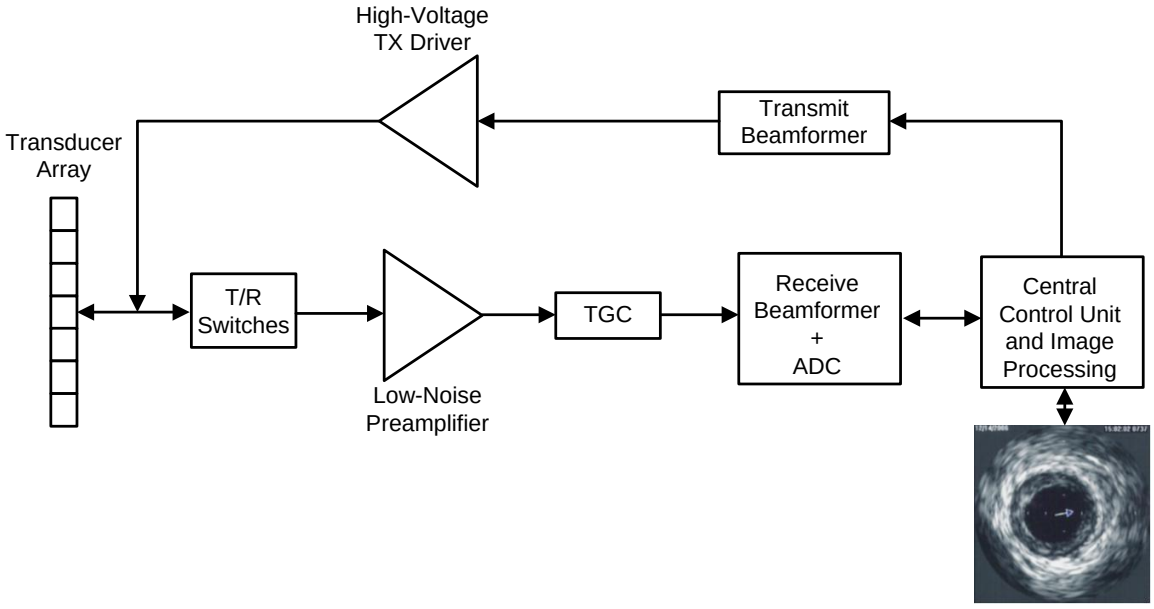


Figure 22. Block diagram of a typical ultrasound front-end system

The first component of the receiver chain is a low-noise preamplifier. Common to all sensor front-end circuits, the first amplifier's noise performance in the receiver path determines the SNR of the entire signal path. Hence, a critical task of the preamplifier design is the minimization of the input-referred electronic noise, while maintaining the

bandwidth of the signal. The receiver chain often also includes a time-gain compensation (TGC) circuit [89]. The transmitted ultrasound signal and the received echoes are attenuated as they propagate in the medium. Thus, the echoes reflected from deeper tissue are weaker than those that are reflected from a similar tissue that is closer, which return sooner. The attenuation of the acoustic energy is roughly exponential with depth at an approximate rate of 0.2 dB/cm/MHz [90]. As a numerical example, the rate of attenuation can be calculated to be 8 dB for a 20-MHz signal for a 1-cm imaging depth. TGC function, which is typically implemented with a variable gain amplifier, is used to compensate for this attenuation of the echo by providing a gain that increases with time for each received signal.

Assuming that time-gain compensation is applied to the received signals, the dynamic range depends on the reflectivity differences of the targets. The upper limit of the dynamic range is determined by the strongest echo. The lower limit of the dynamic range is determined by the minimum detectable signal which is proportional to the total noise of the transducer and front-end electronics. Typically, a 40-dB dynamic range is sufficient for an IVUS application.

The receiver chain also includes an ADC to digitize the received signal for further digital signal processing and display. In systems with relatively few receive channels the ADC can be a part of the receive beamformer unit (digital beamforming). However, for arrays with many elements and especially for catheter based applications, providing dedicated ADCs to all of the receive channels is not practical. Alternatively, ADCs can be placed after the beamformer unit where the beamformer delays are implemented in an analog fashion. For IVUS applications, signal digitization is typically performed in the

main processing unit. On the other hand, for other ultrasound applications the ADCs can be integrated in the probe handle. A study that discusses an ADC design for such ultrasound applications can be found in [91].

Transmit and receive beamformers determine the delay patterns of the transmitted and received signals to create a focused beam to improve the image resolution in the desired focal point. A through discussion of various beamforming approaches can be seen in Chapter 6. This chapter mainly discusses the design considerations for high-voltage transmit pulsers, transmit-receive switches and low noise receive amplifiers.

2.1. High-Voltage Integrated Circuit Design for Transmit Pulsing

2.1.1. High-Voltage Devices in CMOS Technology

High-voltage pulser circuitry is used to actuate the transducers to generate ultrasound waves and is an important component of every ultrasound system. Ultrasound imaging is not the only application that requires high-voltage driving capabilities. LCD display drivers, automotive applications and printer head drivers are a few other example applications that require high voltages much above the standard process supply voltages.

To generate the high-voltage pulses, transistors that can withstand high-voltage values need to be used. Double-diffused MOS (DMOS) [92, 93] and Lateral Diffused MOS (LDMOS) [94, 95] transistors are some examples of high-voltage MOS structures. These are usually implemented using a dedicated high-voltage process such as Bipolar/CMOS/DMOS (BCD) technology. These dedicated processes offer good performance high-voltage transistors. However, the additional buried layers, the need for

many specialized extra lithographic masks and processing steps used in BCD processes significantly increase the fabrication complexity and the cost.

Recently, the trend towards reducing the system cost and reducing the form factor favored the use of other lower cost processes such as High-Voltage CMOS (HV-CMOS) [96]. In these processes the existing low-voltage process is modified to add few extra masks to implement the high-voltage devices. These hybrid HV-CMOS processes incorporating high-voltage transistors along with standard low-voltage devices are offered by many existing silicon foundries such as XFAB, TSMC, DALSA Semiconductor or AMS. These processes are simpler and less costly compared to fully-dedicated HV processes; however they still require few extra processing steps, which again is more costly compared to standard processes.

The most cost-effective approach to get high-voltage devices is to use the standard low-voltage CMOS technology and to modify the layout of regular devices to get high-voltage elements [97-99]. This is the lowest cost solution because it is completely compatible with the fabrication process of low voltage devices and doesn't require any additional masks or fabrication steps.

Carefully considering the underlying breakdown mechanisms in MOS transistors is important to design a device with a high breakdown voltage. There are mainly two breakdown mechanisms for an NMOS. First one is the oxide breakdown which occurs when high voltages are applied between the gate and the underlying substrate. Therefore to prevent the oxide breakdown, a field oxide should be applied under the gate area close to the high-voltage node to protect the gate from the high electrical field. The second mechanism is the junction breakdown. Junction breakdown tends to occur on the p-n

junction area close to the surface where the electric field is at its maximum due to the high depletion region curvature. Providing a lightly-doped n-well region between drain and gate creates a drift path and removes the high electric field at the surface and prevents surface breakdown. For that case, breakdown occurs at the bulk between the n-well and the p-substrate which happens at much higher voltages. The high voltage structure that uses the above techniques is called as Extended Drain MOS (EDMOS). Cross-sectional view of the layout of an Extended Drain NMOS can be seen in Figure 23.

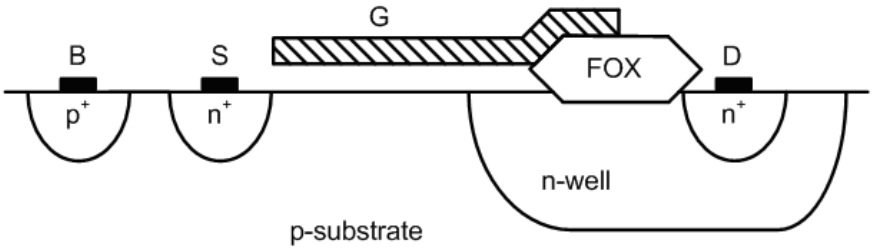


Figure 23. Extended Drain NMOS structure

2.1.2. High-Voltage Pulse Driver Circuits

For ultrasound systems, high-voltage pulses are traditionally provided off-chip using discrete components [100, 101]. However, since the monolithic integration of the transducer arrays and the electronics is more desirable, various techniques of generating high-voltage pulses on chip have been investigated. A standard architecture for an ultrasound pulser (driver or also referred as transmitter) that generates a unipolar pulse is shown in Figure 24. More sophisticated systems may implement bipolar or multilevel pulses.

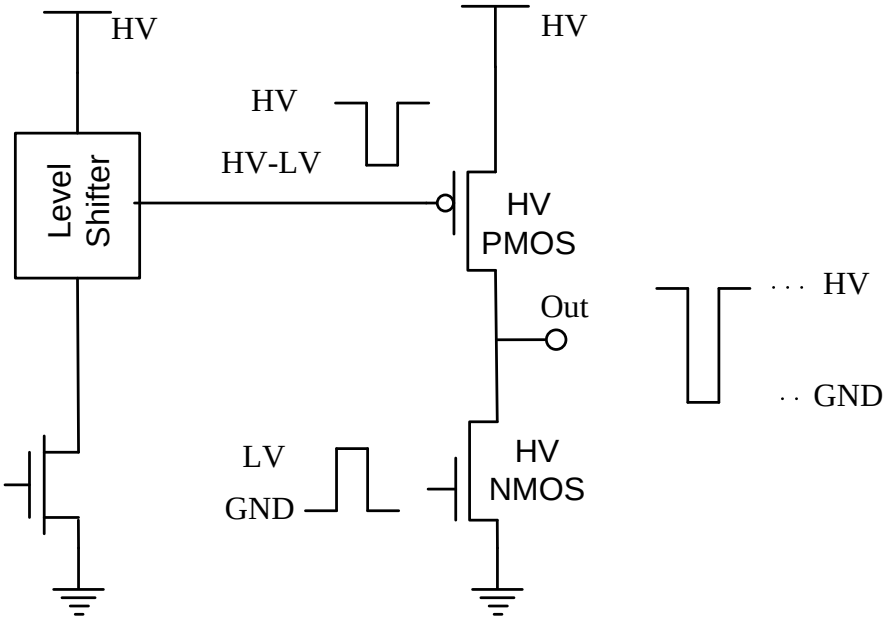


Figure 24. Conceptual schematic of a high-voltage pulse-driver circuit and its control signals.

The gate voltage of the output high-voltage PMOS is provided by a level shifter that takes the transmit trigger signal and shifts it up to refer it to the high voltage (HV). This is required to limit the gate-to-source voltage of the HV-PMOS transistor within the safe sustainable operation voltage, which is determined by the gate-oxide thickness of the device. The level shifter can simply be a resistor [102] or a diode-connected load [103]. Another level shifting approach uses cross-coupled PMOS transistors [92, 104-106]. The approach in [20] combines the level shifting and the high-voltage output stages in a single stage.

It is possible to generate the high-voltage supply required for the pulse driver circuit on-chip using a switch-mode dc-dc boost converter [107] or using a charge pump circuit [92, 108, 109]. For instance, the work in [109] shows a 6-stage charge pump to achieve 19.6 V in 0.35 μm SOI-CMOS. The capacitive charge pump approach does not

require an inductor and therefore for a catheter-based application it is a more feasible approach compared to the inductive boost technique.

2.2. Transmit-Receive Switch

When the same transducer element is used both as a transmitter and a receiver, the transmitter and receiver circuitries share the same node. Thus, there is a need for a switch to isolate these circuitries and protect the low-voltage receive circuitry from the high-voltage transmit pulses. A traditional implementation of transmit-receive protection based on a limiter-expander diode circuitry is shown in Figure 25 [110, 111].

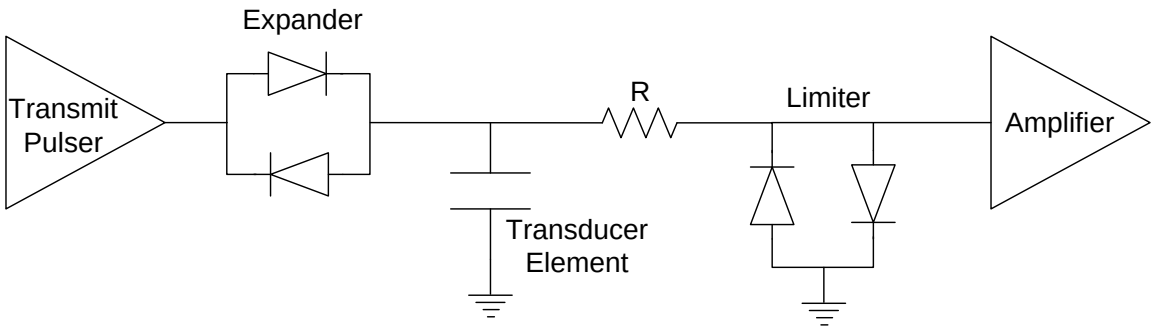


Figure 25. Block diagram of the conventional limiter-expander diode protection scheme

During receive mode the limiter diodes allow low-amplitude echoes to pass unaffected. During the transmit mode, the limiter diodes conduct and clamps the amplifier input to a diode voltage drop. This protects the receive amplifiers getting damaged from the high-voltage pulses during the transmit mode. A resistor (R) is needed to limit the amount of current flowing through the diodes in the transmit cycle. Most of the high-voltage pulse drops on this resistor. The sizing of this resistor is a design

consideration. The resistor value cannot be very small because that would require a large current flow. On the other hand, a large resistor value adds more noise to the system.

During transmit mode the expander diodes conduct and the pulser is connected to the transducer. During the receive cycle the expander diodes isolate the pulser from the received small-amplitude signals. If the output impedance of the high-voltage pulser is sufficiently high during the receive mode, then these diodes can be omitted and the pulser output can be directly connected to the transducer [102, 112].

It is also possible to use a MOSFET switch in place of diodes (Figure 26) [106, 113, 114]. One drawback of this approach is that the switches require active control signals. The switch transistors should be high-voltage transistors and the large size of the high voltage switches may contribute significant parasitic capacitance to the preamplifier input node. Similarly, the on-chip diodes and resistors in Figure 25 also load the preamplifier input node. In both methods, the input loading degrades the noise performance of the system. Further discussions on the design considerations of transmit-receive switch circuitry can be found in [115-117].

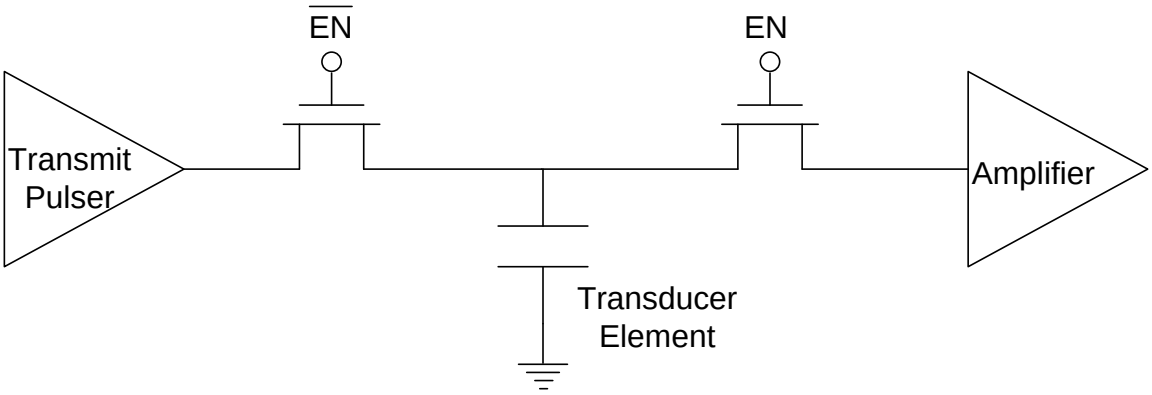


Figure 26. Block diagram of the high-voltage transistor protection scheme

2.3. Overview of Various Preamplifier Configurations for CMUT Sensing

The design of a preamplifier entails many trade-offs between gain, noise, bandwidth, and power dissipation. This section gives an overview of trade-offs of various preamplification approaches for CMUT sensing. As discussed in section 1.3.2, a CMUT element in immersion can simply be modeled with a current source in parallel with a resistor and capacitor [52]. The CMUT equivalent circuit is redrawn here and the capacitive and resistive loading of the preamplifier are shown separately.

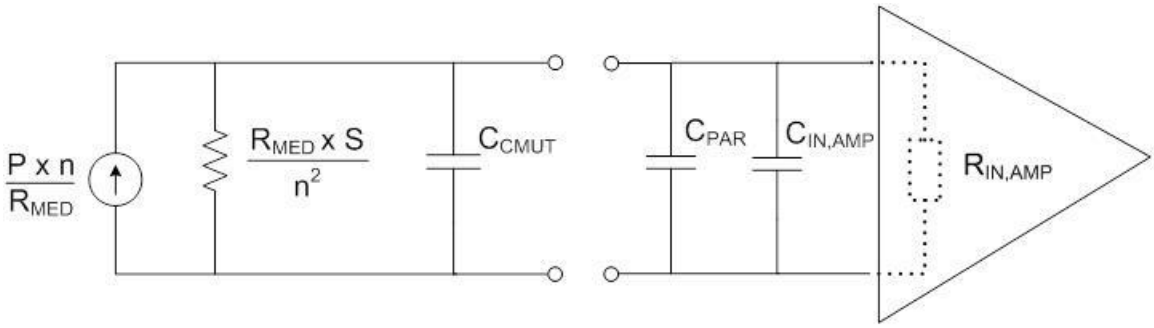


Figure 27. Simplified equivalent circuit of a CMUT in immersion

First assume the case where the amplifier input impedance is infinite, which is typical for open-loop MOS-input amplifiers. It is evident that the total input capacitance (C_{IN}), which includes the capacitance of the parasitic interconnects, the sensor capacitance and the amplifier input capacitance, forms a low-pass filter with the equivalent resistance of the CMUT.

For large transducers the equivalent CMUT resistance can be as small as 100 Ω [60, 118, 119]. For those cases, the roll-off frequency of the low-pass filter is at a very high frequency compared to the frequency band of the transducer and therefore the

transducer-generated signal appears at the voltage amplifier input without any frequency roll-off or degradation.

On the other hand, for tiny transducer elements the equivalent CMUT resistance is much higher compared to the resistance of large transducer elements. For instance, the resistance of a 2D CMUT array element is typically more than 100 kΩ [102, 106] and the resistance value of a CMUT element in a FL-IVUS array can be as high as 1 MΩ [120, 121]. For some numerical calculations assume that the total input capacitance is 1 pF and the equivalent CMUT resistance is 100 kΩ. In that case, the roll-off frequency becomes 1.6 MHz. This implies that at typical IVUS operation frequencies (above 10 MHz) the CMUT current signal integrates over the total input capacitance and generates a voltage at the input of the amplifier that is band limited compared to the wideband CMUT signal.

The band limitation can alternatively be discussed using the expression of the sensed voltage at the amplifier input which can be given as [122]

$$V_{CMUT} = V_{BIAS} \frac{C_0}{C_{IN}} \frac{\Delta d}{d_{eff}} \tag{12}$$

where Δd is the displacement of the membrane, V_{BIAS} is the static bias, C_o is the CMUT capacitance and d_{eff} is the effective gap thickness. It can be seen that the voltage signal at the input of the voltage amplifier is proportional to the average displacement of the membrane. For capacitive devices, displacement decrease with increasing frequency for a given wideband pressure input. In other words, with a wideband pressure signal, the membrane displacement and the sensed voltage will be band limited. This discussion indicates that when used as a preamplifier for a high-impedance CMUT, a voltage amplifier with infinite input impedance [102, 123, 124] would sense the CMUT displacement and would limit the signal bandwidth in immersion. Similarly, a capacitive-

feedback charge amplifier [119, 125-127] integrates the CMUT current over the feedback capacitance and the output again becomes proportional to the displacement of the CMUT [121]. To prevent limiting the CMUT bandwidth, a differentiator circuit can be added after the displacement sensing amplifiers [128, 129]. However, this introduces an additional stage in the receiver chain. For air coupled applications, the signal generated at a particular frequency, i.e. resonance frequency, is sensed so there is no need for wideband operation. For those cases charge or voltage sensing circuits can be used as in [122] which uses source followers.

The above discussions imply that to preserve the bandwidth, the preamplifier for sensing signal from a small CMUT element in immersion should have finite input impedance that is much smaller than the transducer impedance. Since the IVUS array elements are typically small in size, the amplifiers in this thesis are designed as current amplifiers, which by design have low input impedances.

In the following sections various current amplification methods are discussed in detail. The circuit topologies are mainly compared based on their noise performances in CMUT sensing. For fair comparison, the noise performances are compared based on the input-referred noise value, which does not depend on the gain of the amplifier [130]. In section 1.6, various advantages of integrating the preamplifiers close to the transducer array were discussed. So in the arguments henceforward, it is assumed that the preamplifiers are directly connected to the transducer without any cable in between. For the noise performance discussion of the amplifiers, a small FL-CMUT element is considered as the transducer element since that is the most challenging one for the receiver electronics design for the following reasons. Primarily, as mentioned earlier, the

FL-CMUT array element has a very small area which limits its signal level. On top of that, the use of synthetic aperture data acquisition further limits the available signal levels. Additionally, due to its small size and large impedance (on the order of 1 MΩ), FL-CMUT element generates a very low thermal-mechanical noise and therefore it is challenging to design a low noise figure (ideally transducer noise limited) front end receiver for FL-CMUT array elements.

2.3.1. Resistor Termination

A simple way of amplifying CMUT's current output is to terminate the CMUT with a resistor. Typically, the resistor termination should also be followed with a voltage amplification stage before connecting to the buffer that drives the cable. Figure 28 shows a case where the resistor termination (R) is followed with a non-inverting voltage amplifier.

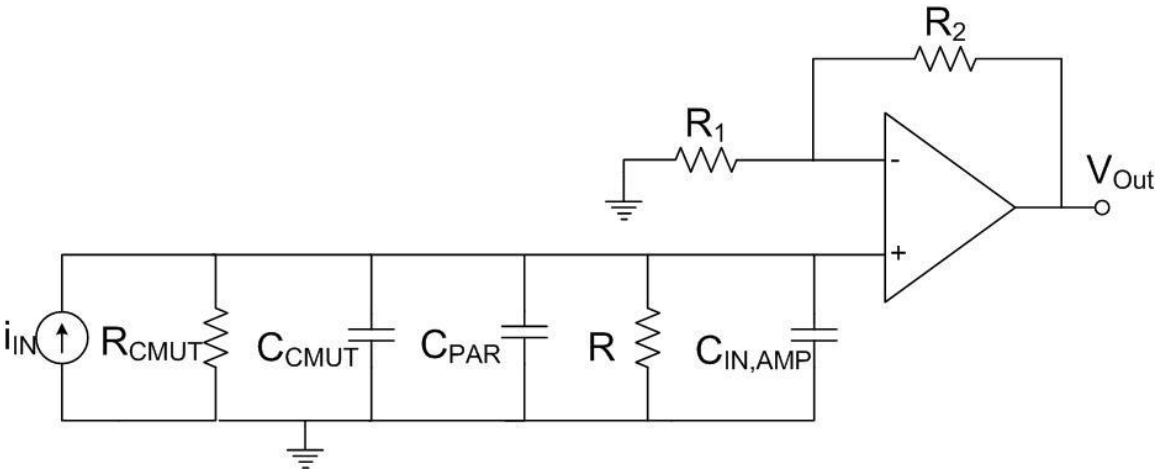


Figure 28. Resistive termination of the transducer followed with a voltage amplifier

The total input capacitance, which includes the amplifier input capacitance ($C_{IN,AMP}$), any parasitic interconnect capacitance (C_{PAR}) and the CMUT capacitance

(C_{CMUT}) is referred as C_{IN} in the following discussions. Assuming that the voltage amplifier has infinite bandwidth and R is sufficiently smaller than R_{CMUT}, the transimpedance gain is given by

$$\frac{V_{OUT}}{I_{IN}}(s) = \frac{(1 + R_2/R_1)R}{1 + sRC_{IN}} \tag{13}$$

where the 3dB bandwidth is clearly expressed as

$$\omega_{-3dB} = -\frac{1}{RC_{IN}} \tag{14}$$

As discussed earlier, the wideband CMUT output should be treated as a current and therefore the input-referred current noise of the front end is of interest. The spectral density of the input-referred current noise can be given as below by only considering the noise of R and the CMUT and neglecting the noise contribution of the core amplifier, R_1 and R_2.

$$\overline{i_{in}^{\,2}} = \frac{4kT}{R_{CMUT}} + \frac{4kT}{R} \tag{15}$$

For a numerical example assume that R_{CMUT} is 1 MΩ and C_{IN} is 1 pF. Assuming a required transducer bandwidth of 20 MHz, a 1 pF total input capacitance limits the resistor termination value to be less than 8 kΩ. The equivalent Johnson current noise of this 8-kΩ resistor is around 1.4 pA/√Hz. On the other hand, the thermal-mechanical noise of a 1-MΩ-impedance transducer is approximately 0.13 pA/√Hz. Using these values, the noise figure for the 8-kΩ termination of a 1-MΩ transducer can be found as 21 dB. In addition, it should be noted that the noise contribution of the core amplifier and the resistances (R_1 and R_2), which are neglected in the above calculation, can easily be comparable to the noise of R. For instance, the LMH6624 (National Semiconductor) used

in [118] has a 2.3-pA√Hz current noise rating, which adds directly to the current noise of R. Therefore, it can be stated that, if the input current and voltage noises of the voltage amplifier that follows the resistor termination are also added to the overall input referred noise, the noise figure of this front-end can easily become much higher than 21 dB. In the next section, it will be discussed that significant improvement in the noise performance can be obtained using a transimpedance amplifier.

2.3.2. Resistor-Feedback Transimpedance Amplifier

Figure 29 shows a schematic of a typical resistive-feedback transimpedance amplifier.

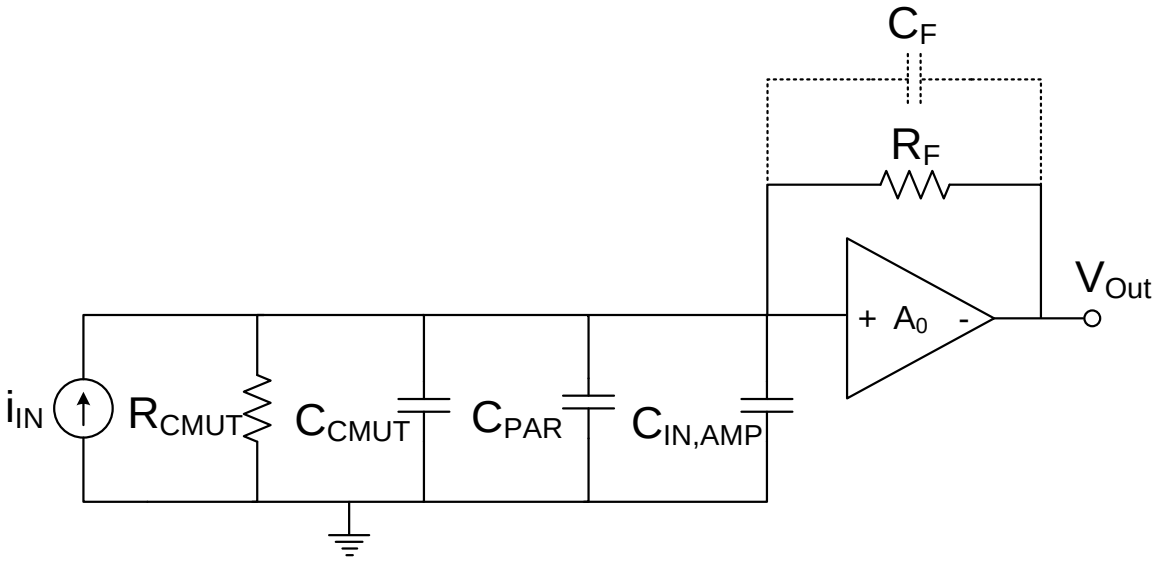


Figure 29. The schematic of a transimpedance amplifier

For the ease of discussion of the noise improvement of the transimpedance amplifier compared to the simple resistor termination, first assume that the core amplifier

has infinite bandwidth and C_F is zero. In that case the TIA has a single pole and the bandwidth is given as

$$\omega_{-3dB} = -\frac{A_0}{R_F C_{IN}}. \tag{16}$$

where A_0 is the open loop gain of the core amplifier. Assuming that the feedback resistance is the dominant source of the noise, the input referred current noise is given as

$$\overline{i_{in}^{\,2}} = \frac{4kT}{R_{CMUT}} + \frac{4kT}{R_F}. \tag{17}$$

Comparing (16) with (14) it can be seen that while maintaining the same bandwidth the value of R_F can be A_0 times higher than the value of a simple resistor termination. Then, comparing (17) with (15), it becomes apparent that compared to the simple resistor termination the amplifier noise performance can be improved by a factor that is proportional to the open loop gain (A_0). Again, for some numerical calculations assume that the required transducer bandwidth is 20 MHz, R_{CMUT} is 1 MΩ, C_{IN} is 1 pF and A_0 is 125. In that case R_F can be as high as 1 MΩ while having a 20-MHz amplifier bandwidth. Considering the thermal-mechanical noise of the 1-MΩ impedance transducer, the noise figure of the system improves to 3 dB, compared to higher than 21 dB noise figure of the simple resistor terminated system. This simple noise and bandwidth analysis of the TIA clearly demonstrates the relative noise advantage of using a TIA over a simple resistor termination. Because of its clear advantages, the resistive-feedback TIA is widely used in current sensing. Some earlier studies that utilize a resistive-feedback transimpedance amplifier for ultrasound sensing applications in particular include front-end electronics for 2D arrays [52] and catheter-based systems based on piezoelectric [44] and CMUT arrays [111, 113, 131].

The above simple noise and bandwidth analysis of the TIA is presented to shortly introduce the relative advantage of using a TIA over a simple resistor termination. However, the actual overall noise improvement of the resistive-feedback transimpedance amplifier depends on the achievable open loop gain, the noise contribution of the core amplifier and the second order effects of the feedback system. To be able to fully understand and evaluate these effects, in the following discussions, more detailed analysis of the circuit shown in Figure 29 is presented in terms of the transfer function and noise characteristics.

It was initially assumed that the amplifier had infinite bandwidth. In the following discussions though, the effect of the finite bandwidth of the core amplifier is taken into account. With a finite bandwidth core amplifier, the TIA transfer function has two poles and is a second order system and the transfer function of the transimpedance amplifier can be given as

$$\frac{V_{OUT}}{I_{IN}}(s) = -\frac{R_F {\omega_N}^2}{s^2 + \frac{\omega_N}{Q} s + {\omega_N}^2}. \tag{18}$$

This second order equation defines the closed loop interaction of two poles, namely the dominant pole of the core amplifier and the pole due to the feedback network. For a complete analysis, this quadratic system should be studied separately for two cases. The first case is without a feedback capacitor and the second case is with a feedback capacitor. Considering the first case and therefore assuming a zero value of C_F, the design equations in (18) can be written as

$$Q = \frac{\omega_N}{\omega_{IN} + \omega_0} \;\; \& \;\; \omega_N = \sqrt{\frac{(1 + A_0)\omega_0}{R_F C_{IN}}} \;\; \& \;\; \omega_{IN} = \frac{1}{R_F C_{IN}}. \tag{19}$$

In these equations ω_o is the bandwidth of the core amplifier. For critical damping and a maximally flat 2nd-order Butterworth frequency response, Q should be set to $\sqrt{2}/2$. With critical damping, the 3dB bandwidth of the TIA is equal to its resonance frequency, ω_N. Assuming ω_{IN} is much smaller than ω_0, it can be found that for critical damping, the 3dB bandwidth of the core amplifier must be $\sqrt{2}$ times the closed-loop bandwidth of the TIA [132]:

$$\omega_0 = \sqrt{2}\,\omega_N \quad where \quad \omega_{-3dB} = \omega_N = \frac{\sqrt{2}A_0}{R_F C_{IN}} \tag{20}$$

Considering the second case and therefore taking the effect of the feedback capacitance (C_F) into account, the design equations are modified as

$$Q = \frac{\omega_N}{\omega_{IN} + \omega_0 + \omega_N{}^2 R_F C_F}. \tag{21}$$

$$\omega_N = \sqrt{(1+A_0)\omega_0\omega_{IN}} \;\&\; \omega_{IN} = \frac{1}{R_F\left(C_{IN} + C_F\right)} \quad . \tag{22}$$

For high values of R_F and C_F the second order response is dominated by the pole due to R_F and C_F and in that case the bandwidth of the closed loop response can be estimated by [20, 133]

$$\omega_{-3dB} = \frac{1}{R_F C_F} \tag{23}$$

For some TIA applications using discrete op-amps, the op-amps are often not designed specifically for the TIA implementation and for those cases a capacitor in feedback (C_F) with an optimized value is used for stable closed-loop operation. It can be seen from (21) that the $\omega_N{}^2 R_F C_F$ term reduces the Q, and helps stabilizing the closed

loop response. The optimum value of C_F that gives a critical damping can be calculated using the below expression [134]

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F \left(C_{IN} + C_F\right)}} \tag{24}$$

With a critical damping case, ω_{-3dB} gets extended by $\sqrt{2}$ times compared to the value in (23) and becomes $\sqrt{2}/R_F C_F$.

On the other hand, for custom designed TIAs, the core amplifier gain and bandwidth can be designed to eliminate the need for an additional stability compensation feedback capacitance. Therefore, for custom designs this shunt capacitance across the feedback is considered as a parasitic capacitance because large values of C_F have a substantial effect on the bandwidth of the TIA and significantly limits the maximum value of R_F that can be implemented. For instance, considering (23) a 50-fF feedback capacitance allows only a 160-kΩ R_F value for a 20-MHz closed-loop bandwidth. Therefore to be able to have a higher R_F value, the parasitic C_F should be minimized.

A schematic of the noise sources including the CMUT element and the receiving TIA is shown in Figure 30.

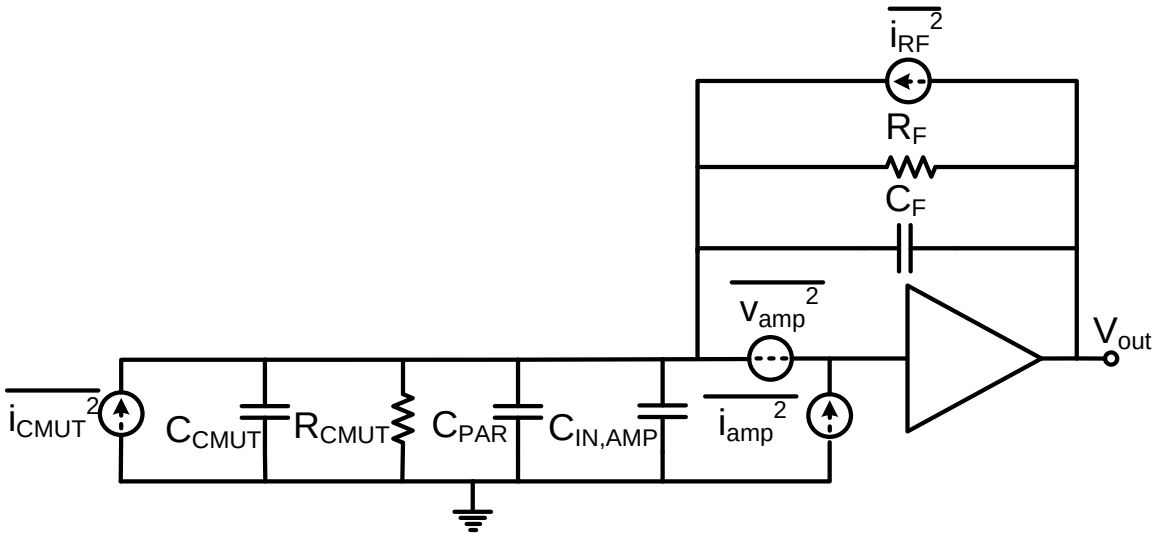


Figure 30. The schematic of the system noise components including the electronics noise and the CMUT thermal-mechanical noise (i_{CMUT}^2) terms.

For this design, the total input-referred current noise is given by:

$$\overline{i_{in}^2} = \overline{i_{amp}^2} + \frac{\overline{v_{amp}^2}}{\left(R_{CMUT} // R_F // C_{IN,EXT}\right)^2} + \overline{i_{RF}^2}, \tag{25}$$

where $C_{IN,\,EXT}$ is the sum of the capacitances external to the core amplifier, including the CMUT capacitance, the parasitic capacitance at the input (C_{PAR}) and the feedback capacitance (C_F). $\overline{i_{RF}^2}$ represents the thermal noise of the feedback resistor (R_F). $\overline{i_{amp}^2}$ and $\overline{v_{amp}^2}$ are the input equivalent current and voltage noise sources of the core amplifier that can be expressed as

$$\overline{i_{amp}^2} = \omega^2 C_{IN,AMP}^{\,2} \frac{\overline{i_d^2}}{g_m^{\,2}} \quad \& \quad \overline{v_{amp}^2} = \frac{\overline{i_d^2}}{g_m^{\,2}}, \tag{26}$$

where g_m is the transconductance, $C_{IN,AMP}$ is the capacitance, and i_d^2 is the current noise of the input transistor that dominates the core amplifier noise. The total input referred

current noise expression including all the capacitances connected to the input can then be expressed as [135]

$$\overline{i_{in}^{\,2}} = \omega^2 \left(C_{IN,AMP} // C_{PAR} // C_F // C_{CMUT}\right)^2 \frac{\overline{i_d^{\,2}}}{g_m^{\,2}} + \frac{1}{\left(R_{CMUT} // R_F\right)^2} \frac{\overline{i_d^{\,2}}}{g_m^{\,2}} + \frac{4kT}{R_F} + \frac{4kT}{R_{CMUT}} \quad . \tag{27}$$

Figure 31 illustrates the input referred noise terms of the TIA given in (27) with frequency. It can be seen that the up to a certain frequency the feedback resistance noise dominates and at higher frequencies the core-amplifier related noise term dominates. Similarly, Figure 32 shows the output referred noise terms of the TIA, indicating that the output voltage noise is shaped by the closed loop TIA response.

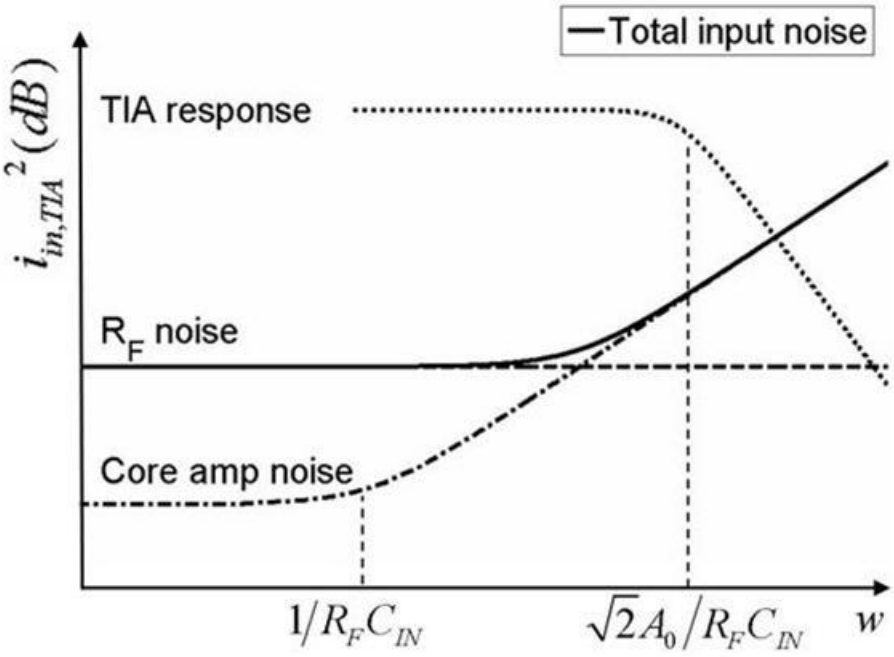


Figure 31. Theoretical input-referred noise terms for the transimpedance amplifier.

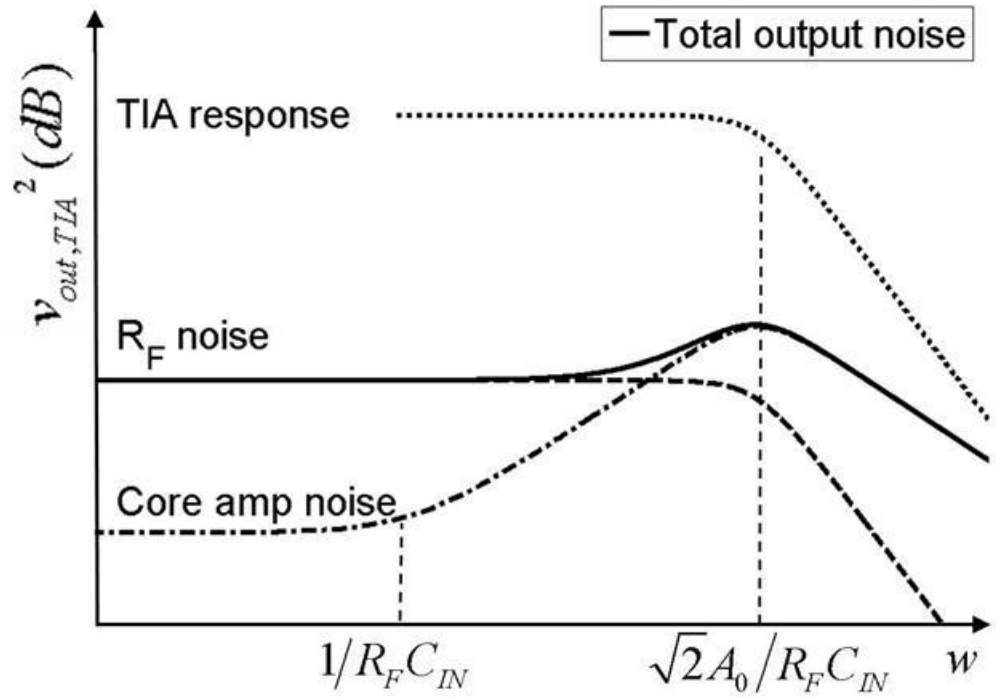


Figure 32. Noise contribution of the feedback resistor (R_F) and the core amplifier on total output noise. Noise terms are shaped by the TIA closed loop response. Output noise depicts a 20dB per decade roll off after TIA's cut-off frequency.

2.3.3. Common-Gate Transimpedance Amplifier

An alternative configuration to sense current signals is a common-gate amplifier [136-138]. The schematic diagram of a common-gate (CG) TIA is shown in Figure 33. In this figure all the capacitances in the input are lumped into a single capacitance and presented with C_{IN}.

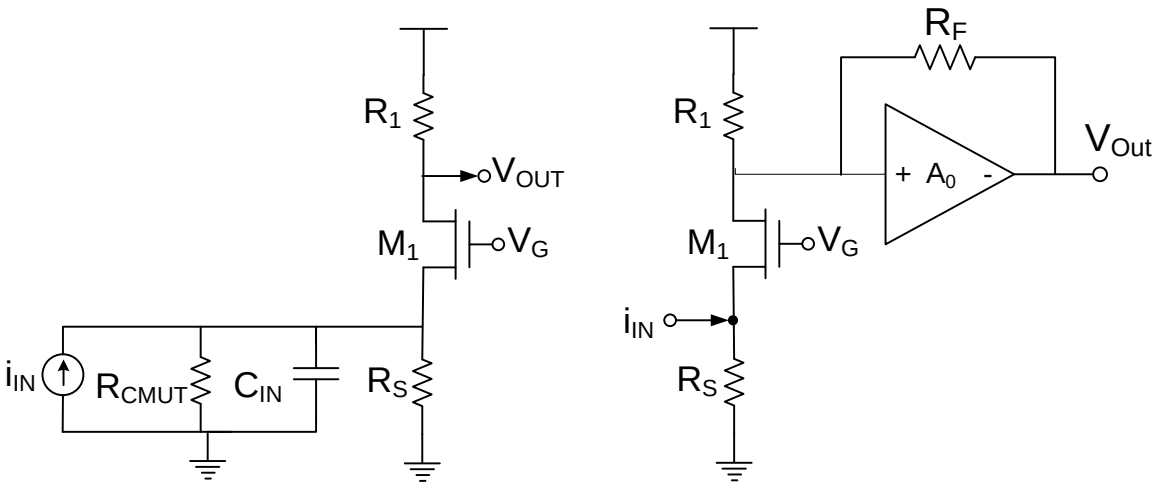


Figure 33. Common-gate input stage (left) and the CG-TIA (right)

Neglecting the second order effects such as the body transconductance and the effect of R_1, the input resistance of the common-gate stage can be assumed to be $1/g_{m1}$. Assuming that $1/g_{m1}$ is much smaller than R_S and R_{CMUT} the transfer function of this circuit is given as

$$\frac{V_{OUT}}{I_{IN}}(s) = -\frac{R_1}{\left(1 + s\frac{1}{g_{m1}}C_{IN}\right)\left(1 + sR_1C_{LOAD}\right)} \tag{28}$$

where C_{LOAD} denotes the capacitance at the output. Typically, $1/g_{m1}$ is small enough that the pole at the source of M1 is non-dominant compared to the dominant pole at the drain of M1 for high values of R_1 and a large capacitance of M1. Usually to extend the bandwidth of the CG stage and to further amplify the signal, a resistive-feedback transimpedance gain stage with low input impedance is included following the common-gate input stage (Figure 33-right). The main advantage of the CG input stage is that it acts as a current buffer and decouples the sensor capacitance from the dominant pole. This relaxes the effect of the large input capacitance from determining the bandwidth. To

provide even more enhanced decoupling of the sensor capacitance a regulated-cascode input structure can be used [103, 139]. Since the common-gate input stage decouples the bandwidth from the sensor capacitance; the stability and bandwidth can be maintained for a variety of input capacitance values. Therefore, this CG-TIA topology can be preferred as the preamplifier for applications where a single amplifier needs to be used to interface with sensors that can have a wide range of capacitance values.

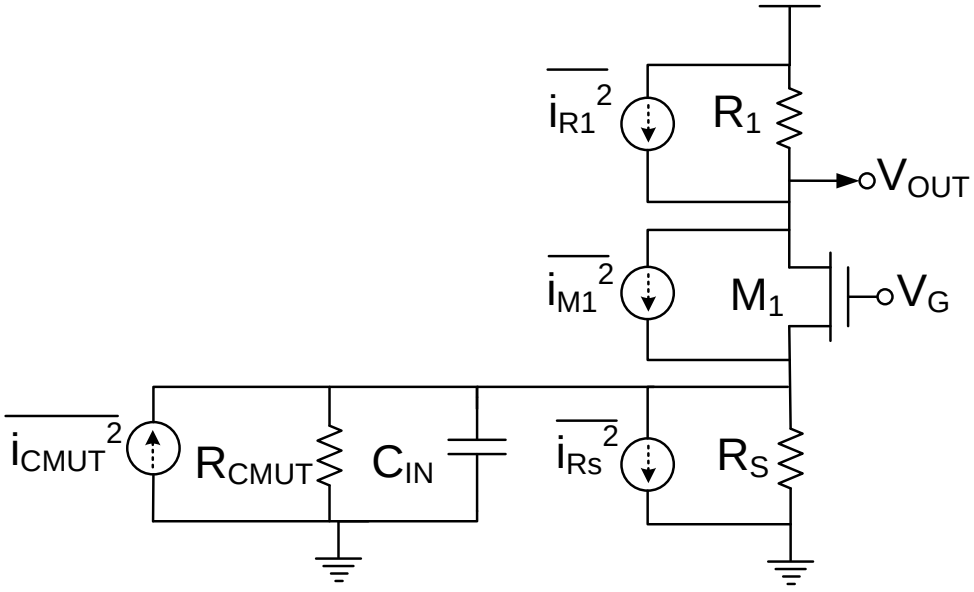


Figure 34. The schematic of the system noise components of the common-gate input stage

Figure 34 shows the equivalent noise model for the common-gate input stage. The spectral density of the equivalent input-referred current noise can approximately be given by [132, 136]

$$\overline{i_{in}^2} = \frac{\omega^2 C_{IN}^2}{g_{m1}^2}\left(\overline{i_{M1}^2} + \frac{4kT}{R_1}\right) + \frac{4kT}{R_S} + \frac{4kT}{R_1} + \frac{4kT}{R_{CMUT}} \tag{29}$$

Note that the current noises of R_S and R_1 are directly referred to the input noise. On top of that, the current gain of the common gate stage is unity; consequently although

not explicitly shown in (29), the current noise from any subsequent stages gets also directly reflected to the input. Therefore, in practice, the resistor-feedback transimpedance amplifier that follows the common-gate input stage might introduce significant noise as well. One should note that in (29), the noise term related to R_1 is analogous to the noise of R_F given in (27). It is clear that the value of R_1 should be maximized to minimize its noise contribution. However, the value of R_1 is limited by the available voltage headroom for R_1 and the value of the bias current through M1, which is typically kept large to increase g_{m1} to reduce the input-referred noise. As a numerical example, assume a 100-µA bias current and a 2-V voltage headroom. In that case, the value of R_1 gets limited to 20 kΩ. As a comparison, in the resistive feedback topology, R_F does not carry a bias current and therefore its value can be maximized without any voltage headroom concerns. However, for very high frequency applications and/or the cases where the input sensor capacitance is large, the R_F value for a resistive-feedback TIA would be significantly limited as well. For instance again as a numerical example assume a 10-pF sensor capacitance, an operation frequency of 1 GHz and a core amplifier gain of 100. In that case the R_F value in a resistive-feedback TIA would be limited to 1.6 kΩ. Therefore, for cases where the value of R_F is significantly limited, the CG-TIA approach can have a better noise performance compared to the resistive-feedback TIA given that the amount of the added extra noise of R_S and the following stages do not negate the noise improvement. On the other hand, for instance for the FL-IVUS application where the sensor capacitance is less than a pF and the operation frequency is on the order of 20 MHz, the R_F value can be made quite large (i.e. in the MΩ range). In that case, the resistor-feedback TIA offers significantly less noise compared to the CG-TIA. Another disadvantage of the common-gate topology is that the common-gate input stage followed

by another transimpedance stage consumes more area and more power compared to a single-stage resistive feedback approach.

2.3.4. Capacitive-Feedback Transimpedance Amplifier

Another receiver architecture that is used for CMUT sensing in this thesis is based on a capacitive feedback approach (Figure 35). This alternative receiver architecture is introduced first in [140] and further discussed in [141]. This architecture is promising for low-noise detection because it does not use a noisy resistor in the feedback network. This circuit mainly implements a current amplification to generate I_{OUT} which gets multiplied by R_D to obtain a voltage output.

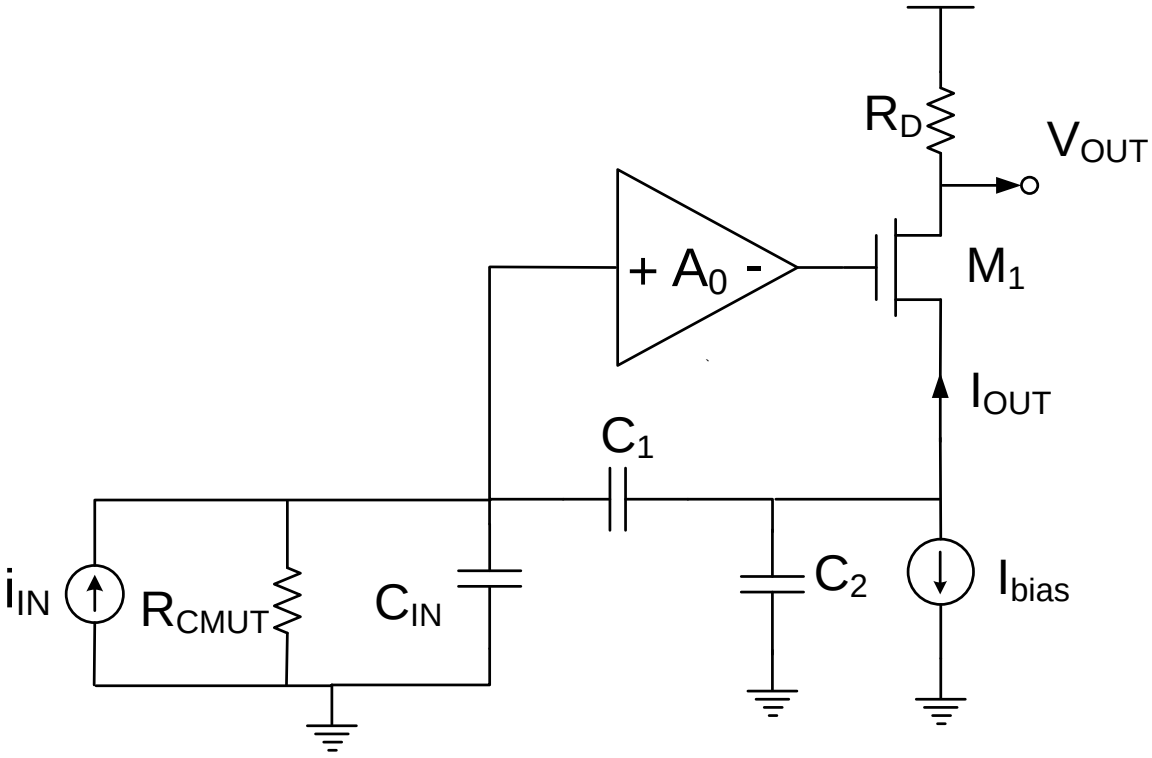


Figure 35. Schematic of the capacitive-feedback transimpedance amplifier.

For the below analysis, for simplicity, it is assumed that at the frequencies of interest, R_{CMUT} can be neglected compared to the impedance of C_{IN}. A numerical example using the previously considered 1-pF C_{IN} and 1-MΩ R_{CMUT} values can be used to support this assumption. At 10 MHz, a 1-pF C_{IN} has approximately 16-kΩ impedance value, which is much smaller than the 1-MΩ CMUT resistance. Furthermore, for larger CMUTs with smaller R_{CMUT} values, the CMUT capacitances would also be larger which would increase the C_{IN} value. This implies that the assumption to neglect R_{CMUT} compared to C_{IN} at typical CMUT operation frequencies should also hold for large CMUT elements.

A detailed analysis of the feedback system in Figure 35 yields the following transfer function:

$$\frac{i_{OUT}}{i_{IN}}(s) = \frac{sC_1 + (C_1 + C_2)A_0\omega_0}{s^2 A + sB + C}, \tag{30}$$

where

$$A = \frac{(C_1 + C_2)(C_{IN} + C_2) - C_1^{\,2}}{g_{m1}} \quad and$$

$$B = \frac{(C_1 + C_2)(C_{IN} + C_1)\left(\omega_0 + \frac{g_{m1}}{(C_1 + C_2)}\right)}{g_{m1}} \quad and \tag{31}$$

$$C = C_1 A_0 \omega_0 + (C_{IN} + C_1)\omega_0$$

In these equations, g_{m1} is the transconductance of M_1; ω_o and A_o are the bandwidth and gain of the core amplifier. Assuming $C_1A_0 >> C_{IN} + C_I$ and $C_2 >> C_1$ the expression in (30) can be simplified as

$$\frac{i_{OUT}}{i_{IN}}(s) = \frac{\frac{C_2}{C_1}\left(1+\frac{s}{\frac{C_2}{C_1}A_0\omega_0}\right)}{1+\frac{s}{\omega_N Q}+\frac{s^2}{\omega_N{}^2}} \tag{32}$$

where

$$\omega_N{}^2 = \frac{C_1 A_0 \omega_0 g_{m1}}{(C_1 + C_{IN})C_2} \;\; and \;\; Q = \frac{\omega_N}{\omega_0 + \frac{g_{m1}}{C_2}} \tag{33}$$

The transfer function in (32) exhibits a zero but it is at a relatively high frequency and can be neglected. To analyze the behavior of this second-order system first assume a dominant-pole case where the transfer function is written as

$$\frac{i_{OUT}}{i_{IN}}(s) = \frac{1}{\frac{s^2}{\omega_{dom}\omega_2} + s(\frac{1}{\omega_{dom}}) + 1} \tag{34}$$

where

$$\omega_{dom} = \frac{C_1 A_0 \omega_0 g_{m1}}{C_2(C_{IN} + C_1)\left(\omega_0 + \frac{g_{m1}}{C_2}\right)} \;\; and \;\; \omega_{dom}\omega_2 = \frac{C_1 A_0 \omega_0 g_{m1}}{(C_{IN} + C_1)C_2} \tag{35}$$

In this expression w_{dom} represents the dominant pole and ω_2 is the second (non-dominant) pole of the closed-loop system. Now further assume that $\omega_0 >> g_{m1} / C_2$. In that case the 3dB bandwidth and the non-dominant pole of the system can be given as

$$\begin{aligned} \omega_{dom} &= \omega_{-3dB} = \frac{C_1 A_0}{(C_{IN} + C_1)}\frac{g_{m1}}{C_2} \\ \omega_2 &= \omega_0 \end{aligned} \tag{36}$$

Now let's consider the case where ω_0 is higher than g_{m1}/C_2 but it is not high enough that $\omega_0 >> g_{m1}/C_2$ is not valid. It should be noted that to ensure stability, ω_0 should be kept equal to or higher than $\frac{2C_1A_0}{(C_{IN}+C_1)}\frac{g_{m1}}{C_2}$. The core amplifier bandwidth value (ω_0) being equal to $\frac{2C_1A_0}{(C_{IN}+C_1)}\frac{g_{m1}}{C_2}$ is a special case where the Q of the second order system gets equal to $\sqrt{2}/2$ and for that critical damping case the bandwidth becomes

$$\omega_{-3dB} = \sqrt{2}\frac{C_1A_0}{(C_{IN}+C_1)}\frac{g_{m1}}{C_2} \tag{37}$$

A similar analysis can be done for the $\omega_0 << g_{m1} / C_2$ case, which with a similar dominant-pole approximation yields

$$\begin{aligned} \omega_{dom} &= \omega_{-3dB} = \frac{C_1A_0}{(C_{IN}+C_1)}\omega_0 \\ \omega_2 &= \frac{g_{m1}}{C_2} \end{aligned} \tag{38}$$

However, note that this $\omega_0 << g_{m1} / C_2$ case is not desired because it requires having a high g_{m1}, which requires a high value of bias current through M1, which in turn limits the value of R_D and a low value of R_D increases the noise of the system.

The expression in (30) suggests that the current gain of the system at dc is given as $\frac{(C_1+C_2)A_0}{C_{IN}+C_1(1+A_0)}$. If the $C_1A_0 >> C_{IN}$ approximation is valid then the dc current gain becomes simply $1+C_2/C_1$. It follows that the overall transimpedance gain is given by this current gain multiplied by R_D.

From the 3dB expression in (36), it can be seen that the bandwidth does not depend on the value of R_D. This is an important advantage of this amplifier architecture as it does not have the gain-bandwidth tradeoff of the resistive-feedback TIA.

The input-referred current noise is given as

$$\overline{i_{in}^{\,2}} = \frac{1}{\left(1+\frac{C_2}{C_1}\right)^2}\left(\frac{4kT}{R_D}+i_{dbias}^{\,2}\right)+\omega^2\left(C_{IN}+C_1\right)^2\frac{\overline{i_d^{\,2}}}{g_m^{\,2}} \tag{39}$$

where g_m is the transconductance, and i_d^2 is the current noise of the input transistor of the core amplifier that dominates the core amplifier noise. Similarly, i_{dbias}^2 represents the current noise of the current bias circuitry that provides the bias current (I_{bias}) for M1. Although, not shown in (39) explicitly, M1 also contributes some noise. However, the voltage noise at the gate of M1 gets divided by the large A_0 value while getting referred to input and therefore noise of M1 can be neglected. From (39) it can be seen that the current noise terms of the bias circuitry and the load resistance (R_D) gets divided by the current gain when referred to input, which is advantageous to get a low input-referred noise. On the other hand, note that the second noise term in (39) which is proportional to the core-amplifier voltage noise term also exists in the resistive-feedback noise equation in (27). Therefore, for applications where the core-amplifier noise dominates the overall noise, the capacitive-feedback architecture would have a similar noise performance compared to the resistive-feedback TIA. However, for low frequency applications, where it is more likely that the feedback noise of the architecture dominates the overall noise, the capacitive-feedback TIA may offer much reduced noise levels compared to the resistive-feedback TIA. Especially for large capacitance transducers, the R_F value for a

resistive feedback cannot be very high, which increases its current noise contribution. Therefore, for instance as a preamplifier for low-frequency and high-capacitance 1D arrays, this capacitive-feedback architecture seems promising.

CHAPTER 3

FRONT-END RECEIVER ELECTRONICS FOR MONOLITHIC CMUT-ON-CMOS IMAGING ARRAYS

In order to implement a low-cost, high-performance silicon-based IVUS imaging device, integration of optimized frontend electronics and CMUT transducer array elements on a single chip is critical. Forming the sensor elements on the same silicon substrate with the CMOS electronics eliminates the parasitic capacitance due to interconnect between the electronics and CMUT array element which is critical for design of receiver electronics to achieve high SNR from small CMUT elements. This chapter describes the design of CMOS receiver electronics for monolithic integration with CMUT arrays for high-frequency intravascular ultrasound imaging. A custom 8-inch wafer is fabricated in a 0.35-μm two-poly, four-metal CMOS process and then CMUT arrays are built on top of the application specific integrated circuits (ASICs) on the wafer. The advantages of the single-chip CMUT-on-CMOS approach in terms of receive sensitivity and SNR are discussed. Low-noise and high-gain design of a transimpedance amplifier optimized for a forward-looking volumetric-imaging CMUT array element is discussed as a challenging design example. Amplifier gain, bandwidth, dynamic range and power consumption trade-offs are discussed in detail. With minimized parasitics provided by the CMUT-on-CMOS approach, the optimized TIA design achieves a 90-fA/√Hz input referred current noise, which is less than the thermal-mechanical noise of the CMUT element. Successful system operation is shown with a pulse-echo measurement. Transducer noise-dominated detection in immersion is also demonstrated

through output noise spectrum measurement of the integrated system at different CMUT bias voltages. A noise figure of 1.8 dB is obtained in the designed CMUT bandwidth of 10 MHz to 20 MHz.

The specific application considered in this chapter is forward-looking (FL)-IVUS. As discussed earlier a FL-IVUS system would be useful for dealing with chronic total occlusions (CTO) in blood vessels and guiding stent placements. Figure 36 shows the schematic diagram of a FL-IVUS probe with a CMUT array integrated with front-end receiver electronics.

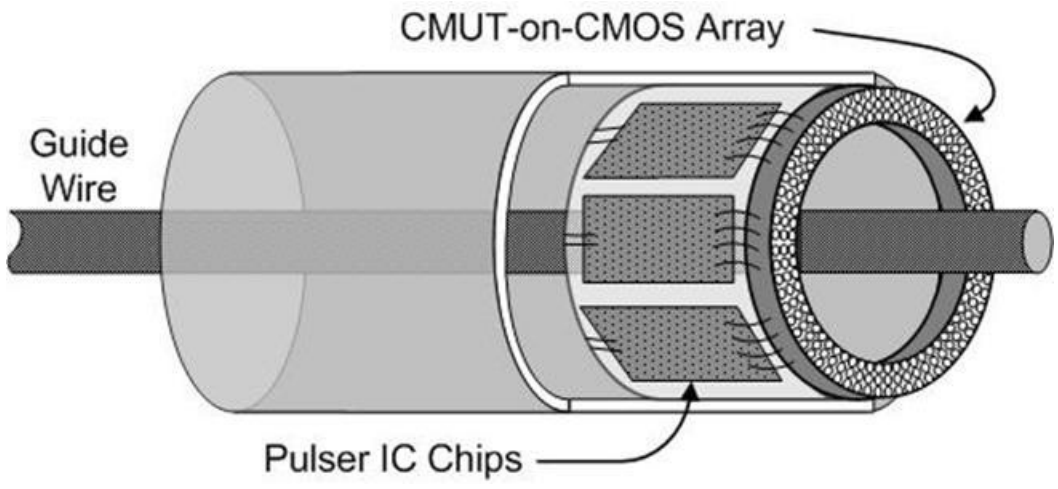


Figure 36. Schematic diagram of a forward-looking IVUS catheter employing CMUT-on-CMOS. The receiver circuitry is monolithically integrated with the CMOS array on the tip of the catheter which minimizes the interconnect parasitics. Transmit circuitry chips may be separate and located on the sides of the catheter.

3.1. Motivation for Monolithic Integration

The parasitic interconnect capacitance is a significant factor degrading the signal-to-noise ratio on the receive side of FL-IVUS array elements with very small capacitances [111, 119]. A method for reducing electrical interconnect parasitics is

through-wafer-via interconnect technology. Using flip-chip bonding to electronics, a total interconnect parasitic capacitance between 100 fF to 500 fF was reported [20]. This hybrid-integration approach allows circuits and CMUTs to be optimized separately; however it requires extra fabrication steps including flip-chip bonding, which increases complexity. Previous efforts of single-chip integration of CMOS and CMUT devices include [142] where a BiCMOS fabrication process with modified steps was used to build CMUTs during electronics fabrication. The main drawback of that approach is that it uses an intermediate CMOS micromachining process and thus alters standard electronics fabrication, which adds extra cost. In addition, transducer design is limited because this approach does not allow any control over gap or membrane thicknesses. One can also use conventional CMOS process flow without modifying the electronics fabrication to build CMUTs where the metal and passivation layers are etched during post-CMOS processing [127, 143, 144]. In these approaches the CMUT design is still limited by the existing foundry procedure. In addition, CMUT elements have to be located on the side of the electronics, which is not acceptable for dense arrays.

A viable approach to mitigate parasitic interconnect capacitances relies on monolithic integration of CMUTs with CMOS electronics where sensor elements are formed on the same silicon substrate with the CMOS electronics [119, 126]. Single chip CMOS-MEMS integration has led to the most successful commercial MEMS devices, such as air bag accelerometers from Analog Devices and digital mirror displays from Texas Instruments. Single chip micromachined gas sensor [145] and accelerometer systems [146] have also been demonstrated in literature. Similarly, for successful implementation of CMUT based miniature arrays for ultrasound imaging like IVUS and

ICE, single chip integration is also very promising. The single chip CMUT-on-CMOS integration eliminates the parasitic capacitance due to interconnect (i.e. wirebond, pad capacitance) between the electronics and CMUT array element. It also significantly reduces the chip-to-chip electrical interconnect problem, increases compactness, enables a smaller die size and reduces cost. In this chapter, a CMUT-on-CMOS approach is reported where CMUT elements are built after the CMOS fabrication and both electronics and CMUT designs are separately optimized.

3.2. Full CMOS Wafer Design for CMUT-on-CMOS

To implement the monolithic system, a custom wafer in TSMC (Taiwan Semiconductor Manufacturing Co.) 0.35-µm two-poly, four-metal CMOS process is designed and integrated with CMUT arrays using a low-temperature fabrication process [147]. The 8-inch CMOS wafer contains many reticles of size 2 cm × 2 cm that are repeated to fill the wafer (Figure 37). Part of the reticle contains many smaller ASICs that are optimized with significant design effort to meet the specifications for three different CMUT arrays having different bandwidths and geometries designed for IVUS and ICE applications. The number of receive and transmit elements, operation bandwidth and calculated device capacitances of CMUT arrays used in these applications are presented in Table 1.

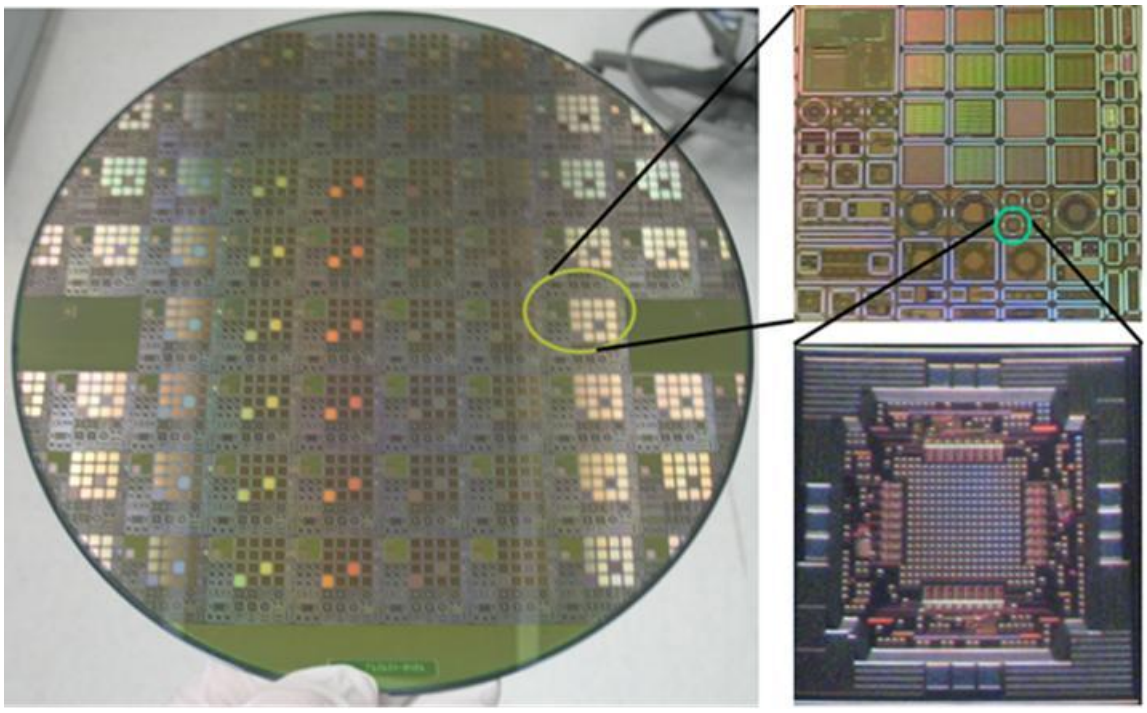


Figure 37. The picture of the 8-inch CMOS wafer fabricated in a 0.35 μm CMOS (left), the picture of the 2 cm x 2 cm reticle (top right) and the 1.5 mm x 1.5 mm chip designed to interface with a forward-looking CMUT array (bottom right).

Table 1. Summary of typical CMUT parameters

	Dual Ring Array	**Annular Array**	**Linear Array**
Number of Elements	32RX – 24TX; 64RX – 48TX	8 RX; 16 RX	64 RX
Operation Freq	10 - 20MHz	10 - 50MHz	3-13MHz
C_{CMUT}	150fF	3pF	5.1pF

This chapter focuses on an ASIC that is custom-designed to interface with a FL-IVUS CMUT array as the advantages of monolithic integration are more pronounced for this particular application. Figure 38 depicts the monolithic integration scheme and the connection to the receiver array through the bottom electrode of the transducer. The design of the full system IC is described and a high-bandwidth, high-gain, low-noise

transimpedance amplifier design that can achieve a noise performance comparable to the transducer noise limit is presented.

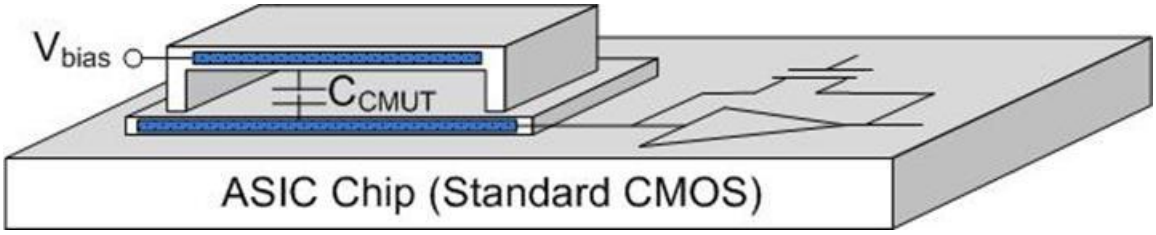


Figure 38. CMUT-on-CMOS monolithic integration scheme. Receive amplifier is connected to the bottom electrode and CMUT is biased with a high voltage DC on the top electrode. Not shown in this figure is an oxide passivation layer between the CMUT bottom electrode and the CMOS ASIC.

3.3. Front-End ASIC for Forward-Looking Volumetric Ultrasound Imaging

Figure 39-left shows a micrograph of an ASIC that is designed to interface with an 800-μm diameter FL dual-ring CMUT array, which includes two rings of CMUT elements [22]. The inner ring includes 24 elements for transmitting ultrasound and there are 32 elements on the outer ring for receiving the acoustic signal. As far as imaging quality is concerned 24TX/32RX configuration is equivalent to the 32TX/24RX configuration when synthetic aperture beamforming is used. The reason to choose 24TX/32RX configuration over the 32TX/24RX configuration is more practical. The IC discussed in this work includes only receiver circuitry and therefore transmit pulses need to be externally connected to the transmit elements in the CMUT array. 32TX/24RX configuration requires 32 connections to the chip for the transmit connections whereas 24TX/32RX configuration requires 24 connections. Therefore, 24TX/32RX is favorable to reduce the required number of connections to the monolithically integrated IC. The post processed IC with the monolithically integrated CMUT array is shown in Figure 39-

right. Array elements are designed with an electrode area of 70 µm x 70 µm. The vacuum gap is 0.12 µm and the thickness of the nitride isolation layers is 0.2 µm. The operation frequency in immersion is between 10 MHz and 20 MHz.

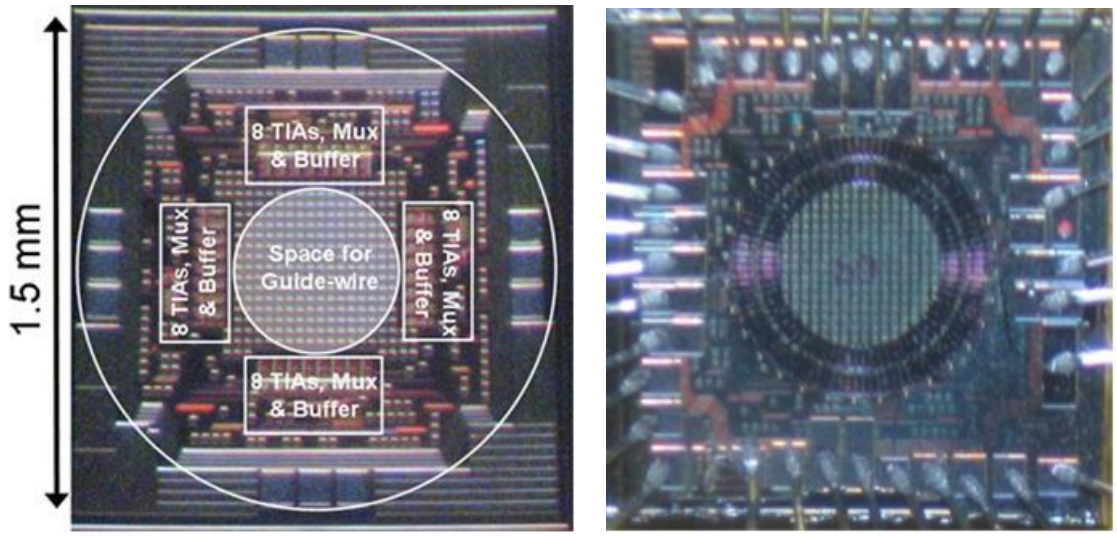


Figure 39. The micrograph of the designed ASIC (left) and the same chip after CMUT post-fabrication (right).

A dedicated low-noise transistor-feedback transimpedance amplifier is provided for each of the 32 receiver elements. The chip includes 4 sets of receiver circuitry, each containing 8 amplifiers. Multiplexing is required for low cable count, which is essential for catheter applications. Therefore each set of the receiver circuitry contains one 8×1 multiplexer. The chip has a total of 4 outputs, one from each receiver array. The operating supply voltage is 3.3 V.

Each receiver set contains a buffer to drive the interconnect cable and scope capacitances, each on the order of 10 pF. We use a push-pull buffer including two source follower stages. In order to not limit the signal bandwidths, the buffer is designed to have a wide bandwidth that is higher than 50 MHz with 50-Ω resistive or highly-capacitive

loads. With a 50-Ω load, the gain of the buffer stage is around 0.25 V/V. Buffer gain value being less than unity does not have a negative effect on system SNR because both signal and noise are affected by this gain. For noise measurements, the buffer output is loaded with the 50-Ω input impedance of the spectrum analyzer so the measured buffer output noise values are reflected to the receive amplifier output by dividing by 0.25. With capacitive loads, the gain of the buffer is around 0.6. The buffer consumes 1 mA of current and covers an area of 35 µm x 50 µm.

The ASIC in Figure 39 fits in a 1.5-mm diameter circular area including all the bondpads. A 500-µm diameter circle at the center is reserved for the guide-wire. There are a total of twelve pins: Four outputs on four sides, one TIA gain tuning voltage, three multiplexer selects, a TIA core amplifier bias, two vdd pins for better power routing and a ground. Additional pads on the CMUT post-fabricated chip are for the two CMUT DC biases for receive and transmit rings and 24 of the connections are for the transmit elements. High voltage transmit pulses are provided externally through those pads. Many small squares seen on the chip micrograph are stacked metal layers that are included for metal fill to meet CMOS density rules and there is no active circuitry under those metal fills. Inputs of the amplifiers are connected to the highest metal (metal 4) that is 15-µm wide. An initial patterning step on the CMOS ASIC is used to create small openings in the passivation layer over these metal 4 amplifier input pads. During the subsequent CMUT fabrication, the bottom electrodes of the receive CMUT elements coat these openings and create an electrical connection to the CMOS amplifiers below.

The layout for the designed circuits is done using the Virtuoso Layout Editor (Cadence Design Systems, San Jose, CA) which generates a gds output file. The CMUT

mask designs are done using AutoCAD program. Therefore, to conveniently transfer the location information for the CMUT connections, the gds file generated by the circuit design tool is converted to an AutoCAD readable dxf file format using a commercial product (LinkCAD).

The layout of the preamplifier TIA used in the ASIC is 40×110 μm^2, which is less than the total area of one transmit-receive pair of CMUT elements so that the receiver circuitry fits under the footprint of the CMUT array. Each TIA consumes 2 mA of current.

We performed pulse-echo experiments in water to verify the functionality of the monolithically integrated CMUT array. The setup for the ultrasonic measurement is illustrated in Figure 40-left. The top electrode of the receiver array is common to all of the elements and the high voltage dc bias is applied to this common top electrode. The receiver element is biased at its top electrode to about 80% of the collapse voltage and the bottom electrode (the electrode closest to the CMOS electronics) is connected to the TIA through the topmost metal layer. The receiver transimpedance amplifier dc input voltage is around 1 V and is much smaller than the dc bias that is applied from the top electrode. The CMUT itself acts as a capacitive block between the high voltage bias and the receive circuitry. All transmit elements also share a single DC bias through a connection to their common top electrode. The bottom electrodes of the transmit elements are connected to external pads to route TX pulses to the CMUT elements. The oxide passivation layer between the CMUT bottom electrode and the ASIC top metal level protects the ASIC from the high voltage pulse.

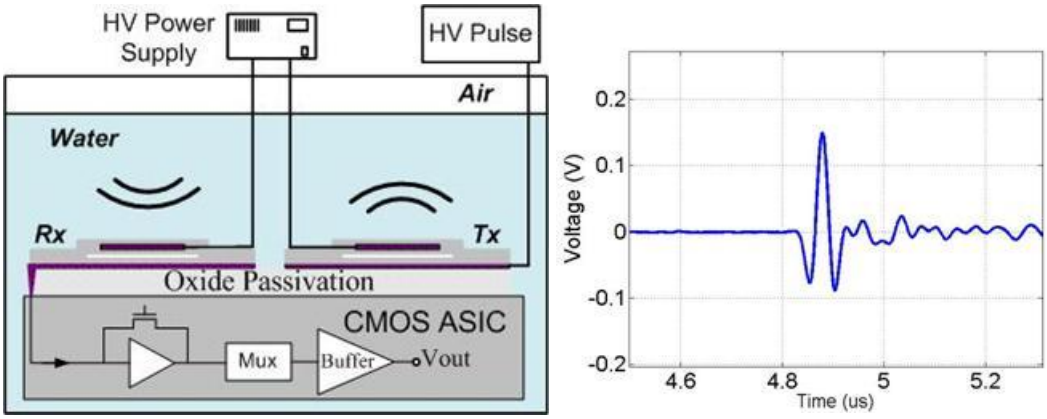


Figure 40. The test setup (left) and a measured pulse-echo response from the monolithically integrated array from the water air interface (right).

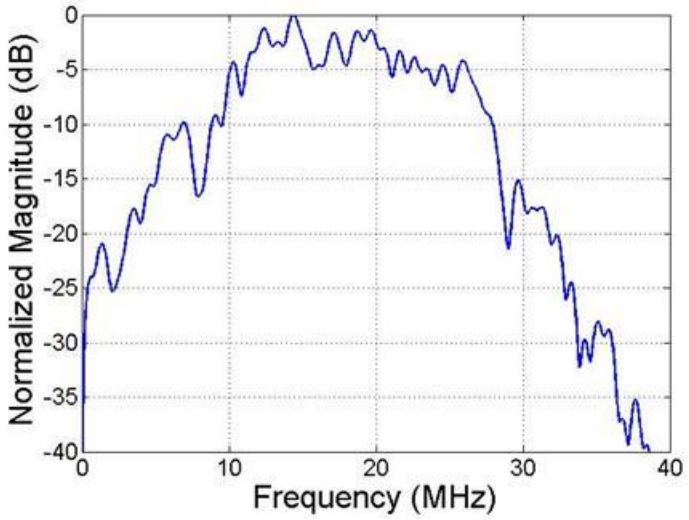


Figure 41. The normalized frequency response of the pulse-echo shown in Figure 40. The center frequency is 15.2 MHz.

The CMUT-CMOS chip was wirebonded on a 40-pin package for testing and the connections were coated with parylene to prevent electrical shorting (Figure 42). One CMUT element from the inner ring was used as a transmitter and an element from the outer ring was used as a receiver. Pulse-echo data is obtained from a plane reflector (the water-air interface) which is 1.6 mm away from the array. A narrow pulse was applied to the bottom electrode of the transmit element. After 4.8 μs, the acoustic signal arrives

from the plane reflector to the CMUT receiver. Figure 40-right shows the echo signal with a center frequency of 15.2 MHz (Figure 41). This basic experiment shows that the monolithically integrated system is fully functional.

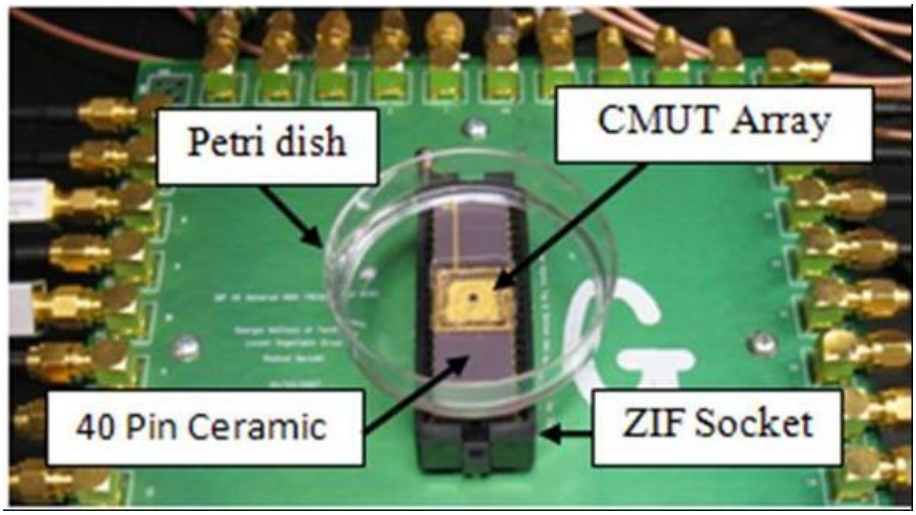


Figure 42. Experimental set up of wire-bonded dual-ring CMUT array in a ceramic package combined with a modified Petri dish. The custom PCB board interfaces the ceramic package to external pulsers, high voltage bias lines, and signal output lines to the digitizer card via SMA connections.

The tail in the echo response is mainly due to the acoustic crosstalk and the ringing in the silicon substrate [17]. The ringing in the echo depends on the thickness of the silicon substrate and is not caused by the CMUT-on-CMOS integration. Similar ringing is seen on other CMUT-on-Silicon papers [17]. The only thickness difference between the CMUT-on-CMOS case and a regular CMUT-on-Silicon case comes from the oxide passivation thickness and that is much smaller compared to the thickness of the silicon wafer. Also, the overall thickness of the CMOS layers on the wafer is 1 micron or so, which is much smaller than any ultrasonic wavelength at the frequency range of CMUT in silicon or in water.

3.4. Transistor-Feedback TIA Design and Core Amplifier Characteristics

A low input impedance transimpedance amplifier with a common-source core stage with shunt feedback for wideband and low-noise performance is implemented in this work. The schematics for the resistor feedback TIA and its full transistor implementation are shown in Figure 43. The gain of the transimpedance amplifier is set by the feedback resistance (R_F). Since larger R_F not only increases the sensitivity of the front-end but also minimizes the noise, a straightforward design approach is to maximize the value of R_F for a given CMUT capacitance while maintaining adequate small signal bandwidth.

The TIA has a low input impedance which is desirable to maximize the received current signal, but not suitable for electrical impedance matching. Electrical impedance matching at the receiver is needed to reduce reflections of the incoming acoustic energy back to the medium that creates imaging artifacts [148] and when a long electrical cable is used between the transducer and the amplifier. For small array elements multiple reflections are not large enough to create imaging artifacts. With the integrated amplifier an electrical cable is not an issue as the buffer after the preamplifier drives the long cable. Therefore, to maximize the received current signal the front end should instead be designed with low input impedance compared to the CMUT element impedance.

Differential input structures are preferred for common-mode noise rejection. An example to a differential input structure amplifier design for CMUT interfacing can be seen in [127]. However, CMUT is inherently a single ended device and the unused differential input side of the amplifier introduces additional input referred noise.

Therefore we implemented the core amplifier with a single ended amplifier to optimize the noise performance.

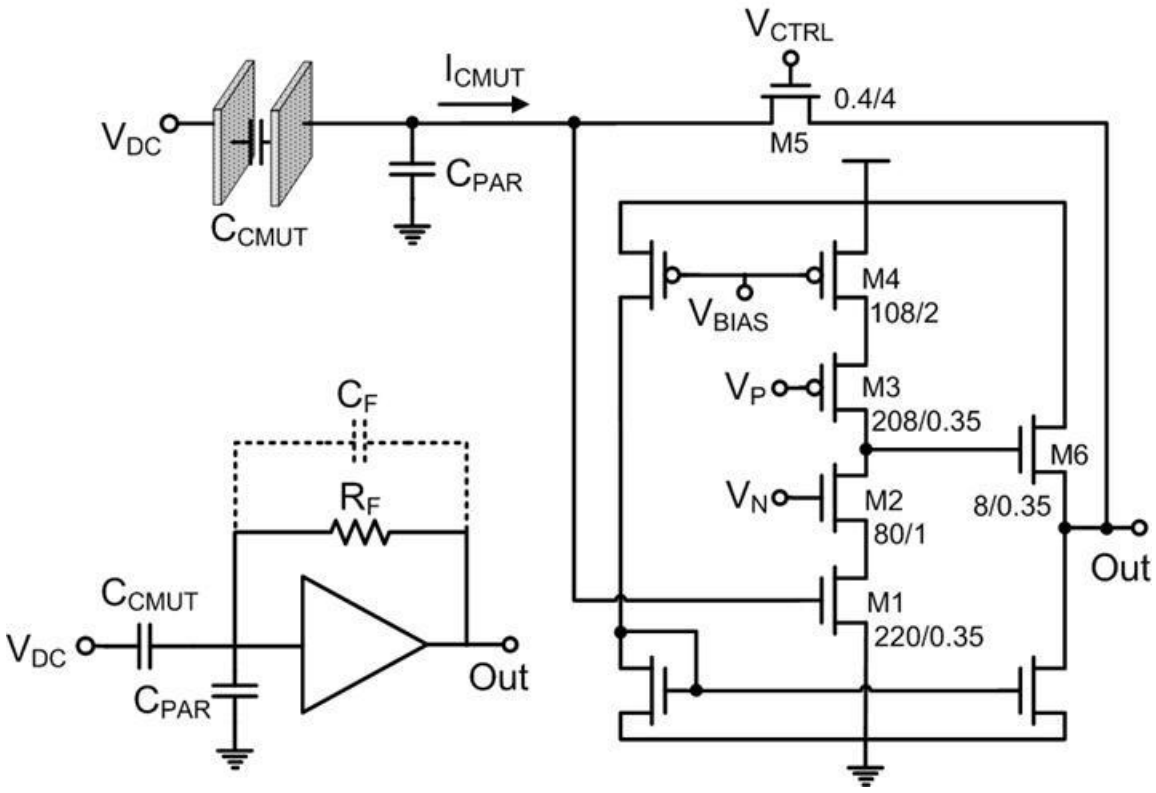


Figure 43. The resistor feedback TIA (left bottom) and the full transistor implementation (right). Transistor dimensions are given in micrometers. Parasitic interconnect capacitance (C_{PAR}) limits the gain of the receiver and increases noise. Monolithic integration improves performance by minimizing C_{PAR}.

TIA designs that implement the feedback resistance with a passive resistor [20] suffer from high values of C_F due to the parasitic capacitances associated with the large area of the polysilicon resistors. In this TIA design, the feedback resistance is implemented using a single long-channel NMOS transistor (M5) in the triode region instead of a polysilicon resistor (Figure 43). The effective resistance value of the triode region feedback transistor is approximated by:

$$R_F = \frac{1}{\mu_N C_{OX} \frac{W}{L}\left(V_{CTRL} - V_{OUT} - V_T\right)}. \tag{40}$$

where μ_N is the carrier mobility, C_{OX} is the gate capacitance per unit area, W is the channel width, L is the channel length and V_T is the threshold voltage of the transistor. V_{CTRL} is the control voltage to tune the closed-loop gain of the TIA. This knob also provides an additional degree of freedom to tune the closed-loop gain and bandwidth of the TIA with respect to process variations and the input capacitance variability. The aspect ratio for M5 is chosen to be W/L = 0.4μm/4μm.

A transistor covers much less area than an equal value on chip resistor, which significantly reduces the layout real estate and reduces the parasitic feedback effects. With careful layout practices such as keeping the input and output traces far from each other on the layout, the parasitic feedback capacitance can be eliminated. In that case, the design equations (19) and (20) that assume no feedback capacitance should be used. In (20) the w_{-3dB} expression indicates a direct trade-off between the input capacitance (C_{IN}) and the maximum R_F value that can be implemented. Therefore any parasitic capacitance at the input should be minimized as it degrades the allowable R_F value. Monolithic integration eliminates this parasitic capacitance and hence enables the use of a higher R_F value.

Based on (20), the core amplifier bandwidth should be tuned to be around 30 MHz to get a desired closed-loop TIA bandwidth around 20 MHz. Also, it can be seen that the gain of the core amplifier should be maximized to obtain the highest R_F and highest sensitivity. In this work to have a high gain, the core amplifier is designed as a cascoded common-source amplifier (Figure 43) and has a simulated open loop gain of

180 when the open loop bandwidth is tuned to 30 MHz. The sizings of the transistors are also noted in Figure 43. The bias current to the core amplifier is controlled with an external connection (V_{BIAS}). The cascode transistor biasing (V_P, V_N) are provided through the on-chip biasing circuitry.

The core amplifier related noise given in (27) is inversely proportional with the transconductance (g_m). To get a higher g_m for a given current value, an NMOS (M1) is used at the input instead of a PMOS device. NMOS has a higher 1/f noise compared to PMOS devices but this noise is effective at frequencies much lower than the CMUT frequency band so minimizing 1/f noise is not a design target. Increasing the bias current increases g_m and hence reduces the voltage noise term. This creates a trade-off between the power consumption and the part of the noise increasing with frequency. Since the objective of this work is to minimize noise as much as possible, the bias current through M1 is designed to be close to a relatively high value of 2 mA. The cascode transistors are designed with a high W/L ratio to increase the gain of the core amplifier and to keep the transistors in saturation. The W/L ratio of M1 was designed to a high value of 220μm/0.35μm to increase g_m. Simulated transconductance (g_m) of the input transistor is 23 mS. The equivalent noise voltage of the core amplifier (v_{amp}) is simulated to be about 1.1 nV/√Hz. The simulated input capacitance for the core amplifier ($C_{IN,AMP}$) is around 400 fF.

3.5. Noise Optimization Enhanced by Monolithic Integration

Optimization of the signal-to-noise ratio (SNR) of the transducer system requires designing receiving electronics that introduce the lowest possible noise for the required

bandwidth. The total input referred current noise expression presented in (27) is repeated here for convenience of the discussion.

$$\overline{i_{in}^{\,2}} = \omega^2 C_{IN}^{\,2} \frac{\overline{i_d^{\,2}}}{g_m^{\,2}} + \frac{1}{\left(R_{CMUT} \,//\, R_F\right)^2} \frac{\overline{i_d^{\,2}}}{g_m^{\,2}} + \frac{4kT}{R_F} + \frac{4kT}{R_{CMUT}}. \tag{41}$$

Inspecting (41), it can be seen that the core amplifier related noise increases with frequency and the rate of increase is proportional to the total capacitance at the input. If the receive sensor element is connected to the amplifier using wirebonding, the parasitic bondpad and wirebond capacitances increase the total input capacitance degrading the noise performance significantly. This effect is more detrimental for small-sized FL-CMUT array elements. Monolithic integration removes all the wirebonding and pad capacitances at the input and results in better noise performance. In addition, as discussed in the next chapter, with reduced total input capacitance, R_F can be designed with values much higher than is possible with wirebonding, which also reduces the input referred noise.

Figure 44 is plotted to investigate the effect of R_{CMUT} on the input referred amplifier noise. Values of two noise terms in (41), namely $\overline{i_d^{\,2}}/g_m^{\,2}/\left(R_{CMUT}\,//R_F\right)^2$ and $4kT/R_F$ are calculated with respect to R_{CMUT}. For this plot R_F is assumed to be 3 MΩ and $\overline{i_d^{\,2}}/g_m^{\,2}$ is assumed to be (1.1 nV/√Hz)^2 based on the simulation values. Plot shows that for R_{CMUT} values higher than 20 kΩ, the $4kT/R_F$ term dominates the $\overline{i_d^{\,2}}/g_m^{\,2}/\left(R_{CMUT}\,//R_F\right)^2$ term. Using the transducer design parameters, when biased close to collapse and in immersion, the FL-CMUT element capacitance and resistance (R_{CMUT}) are calculated to be 150 fF and 1 MΩ, respectively. Therefore it can be stated that the

core amplifier related noise does not depend on the value of R_{CMUT} and the total input referred amplifier noise expression in (41) can be rewritten as below by safely ignoring the $\overline{i_d^{\,2}}/g_m^{\,2}/\left(R_{CMUT}//R_F\right)^2$ term:

$$\overline{i_{in}^{\,2}} \approx \omega^2 C_{IN}^{\,2} \frac{\overline{i_d^{\,2}}}{g_m^{\,2}} + \frac{4kT}{R_F} + \frac{4kT}{R_{CMUT}} \tag{42}$$

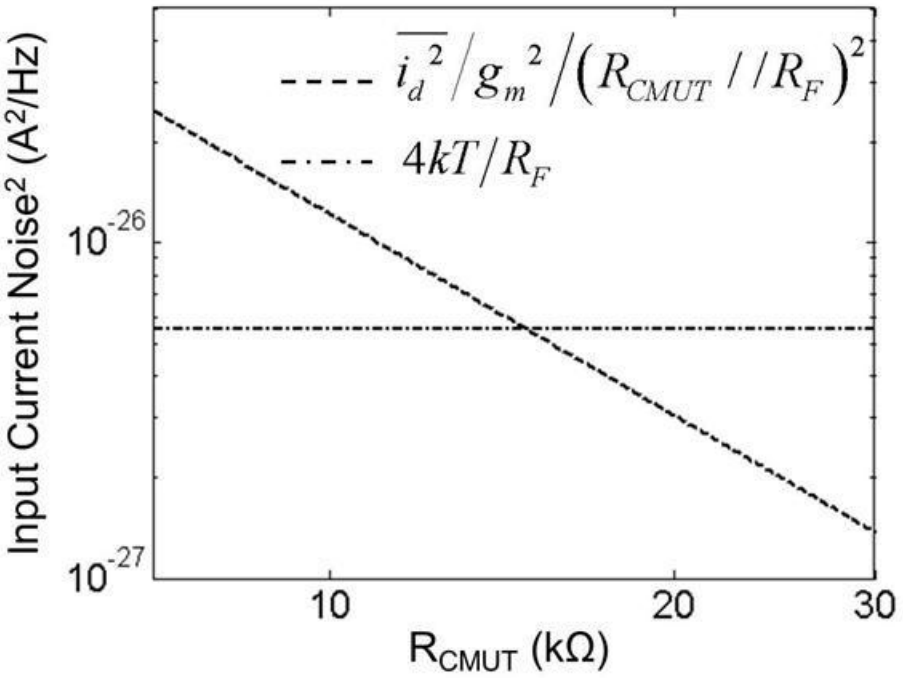


Figure 44. The two noise terms in (41) with respect to R_{CMUT}. The y-scale is drawn in log scale. This plot shows that for higher R_{CMUT} values the total noise does not depend on the CMUT equivalent resistance.

For comparison purposes with other preamplifier designs or to estimate the noise performance that can be achieved with other transducers, one might be interested in the equivalent voltage ($\overline{v_{TIA}^{\,2}}$) and current noise sources ($\overline{i_{TIA}^{\,2}}$) for the transimpedance amplifier (Figure 45).

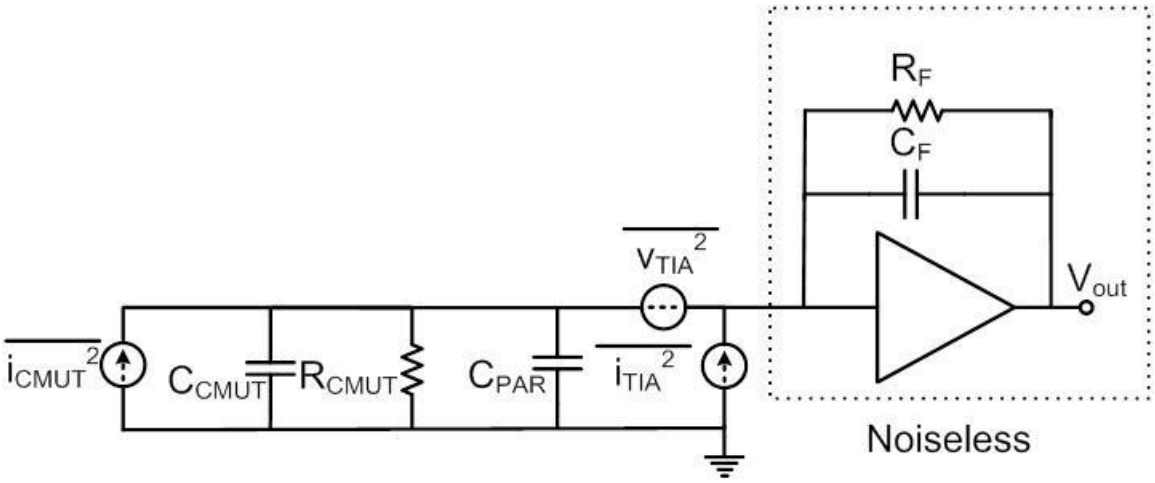


Figure 45. Equivalent representation of the transimpedance amplifier noise with two input noise generators and an ideal noiseless amplifier.

The equivalent TIA noise terms incorporate the noise sources of the core amplifier ($\overline{i_{amp}^2}$ and $\overline{v_{amp}^2}$) and the feedback network. Assuming there is no feedback capacitance, these can be approximated as [149]:

$$\overline{v_{TIA}^2} = \overline{v_{amp}^2} = (1.1\text{nV}/\sqrt{\text{Hz}})^2 \tag{43}$$

$$\begin{aligned}\overline{i_{TIA}^2} &= \overline{i_{amp}^2} + \frac{\overline{v_{amp}^2}}{R_F^2} + \overline{i_{RF}^2} \\ &= \omega^2 (400\,fF)^2 (1.1\text{nV}/\sqrt{\text{Hz}})^2 + \frac{(1.1\text{nV}/\sqrt{\text{Hz}})^2}{(3M)^2} + \frac{1.6\times10^{-20}}{3M} \\ &\approx 85\,fA/\sqrt{Hz}\,@15\,MHz\end{aligned} \tag{44}$$

It can be seen that shunt feedback network does not change the voltage noise and therefore $\overline{v_{TIA}^2}$ term is equivalent to $\overline{v_{amp}^2}$ which is simulated to be (1.1nV/rt-Hz)^2. Equivalent current noise term is higher than $\overline{i_{amp}^2}$ and includes the effect of feedback network noise ($\overline{i_{RF}^2}$). $\overline{i_{amp}^2}$ term is frequency dependent and can be calculated using the

simulated input capacitance ($C_{IN,AMP}$) of 400 fF. $\overline{i_{RF}^{\,2}}$ is related to the feedback resistance which significantly depends on the sensor capacitance.

3.6. Gain and Noise Measurement Results

3.6.1. Transfer Function Testing

Testing the frequency response of a transimpedance amplifier is not a trivial task. A high output impedance current source should be provided at the input of the amplifier. Connecting the output of the network analyzer directly to the input of the amplifier overestimates the bandwidth because 50-Ω output resistance of network analyzer is not high enough compared to the input resistance of the TIA. One way of imitating a current source at the input is to use a large on-chip resistor and convert an input voltage to current over that resistor. An on-chip capacitor can be placed to mimic the CMUT capacitance. For accurate testing, the impedance of the resistor should be much larger than the input resistance of the amplifier so that it can accurately mimic a current source. The simulated input impedance of the designed TIA for a 3 MΩ feedback resistance is found to be 16.5 kΩ. This agrees with the theoretical TIA input resistance which is expected to be equal to the value of feedback resistor over the open loop gain of the core amplifier. The simulated open loop gain of the TIA is 180 and the theoretically expected TIA input resistance is 3MΩ/180 = 16.7 kΩ. Therefore, for accurate testing, the on-chip resistor should have a resistance much higher than 16.5 kΩ. In addition, for accurate testing it is critical to place the passive element that converts voltage input to current on chip [136], which eliminates the effect of pad capacitance in the TIA transfer function.

However, a high value on-chip resistor consumes considerable layout area which results in parasitic capacitances which may affect the bandwidth characteristics of the TIA. Therefore we used an alternative method to measure the transimpedance characteristics, and used the CMUT element itself in series with the TIA to mimic the on-chip high impedance. The test setup can be seen in Figure 46. A voltage signal is applied to the biasing electrode of the CMUT array. The Norton equivalent of a voltage input (V_{in}) in series with the C_{CMUT} is a current source equal to $V_{in} \; x \; 2\pi \; x \; freq \; x \; C_{CMUT}$ and a parallel C_{CMUT}. Therefore the capacitance loading of the CMUT at the TIA input is also included in this measurement. However, this setup does not take into account the increase in the CMUT capacitance when a DC bias is applied to the CMUT element. The capacitance of CMUT with no dc bias is calculated to be around 100 fF. When the CMUT is biased close to collapse the vacuum gap decreases and effective capacitance is calculated to increase to around 150 fF. However, for this small CMUT element a 50 fF capacitance increase is almost negligible because it is an order of magnitude smaller compared to the total capacitance at the TIA input. This test structure is also verified in simulation where a voltage source is connected in series with the CMUT capacitance and an ideal integrator is placed after the TIA output voltage. This simulation setup gives the same transimpedance characteristics when compared to the results of the simulation of the TIA with an ideal current source at the input.

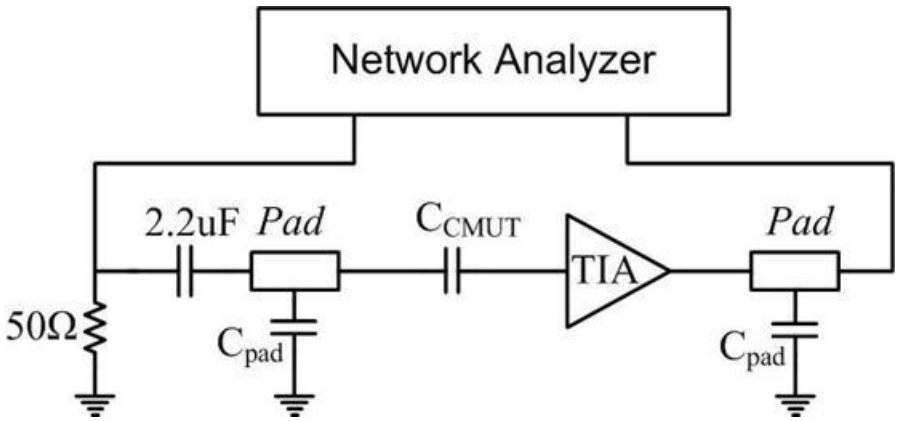


Figure 46. Setup for testing the TIA transimpedance characteristics. The pad capacitance, C_{pad}, does not have an effect on the measured transimpedance because C_{CMUT} is located after the pad.

The simulated transimpedance characteristics for different values of feedback resistance are shown in Figure 47. To be consistent with the electrical measurement, which is discussed next, a 100-fF capacitance is used in simulation to mimic C_{CMUT}. In simulations, there is a 0.3-fF drain-to-source capacitance that is included in the simulation model of the feedback transistor (M5) and it behaves as a feedback capacitor. However, its size is very small and does not impose a substantial damping. In addition, this capacitance is for transistor modeling purposes only and is not a physical capacitance. In the layout of the TIA, the metal connections are routed carefully not to introduce capacitance between the input and output of the amplifier. So, in the real implementation, the effective C_F should be almost zero.

For electrical measurements, one of the outputs of the post processed IC in Figure 39 is connected to an Agilent 4395A and the gain is measured at the buffer output using the equipment in network analyzer mode. Then the measured voltage gain is divided by the buffer gain and multiplied by $1/2\pi x\, freq\, x C_{CMUT}$ to extract the transimpedance gain. Since the dc bias between the CMUT electrodes is very small for this test setup, to extract

the TIA gain from the overall voltage gain measurement, a 100 fF is used as the CMUT capacitance. The transimpedance gain is characterized for different values of feedback resistance and plotted in Figure 48. It can be seen from both the simulation and measurement results that the feedback resistance can be tuned by the control voltage. For increased transimpedance gains, the bandwidth of the TIA drops as expected. Measurement results demonstrate that a 3-MΩ gain can be achieved with a bandwidth higher than 20 MHz. This performance is also supported by the simulation results.

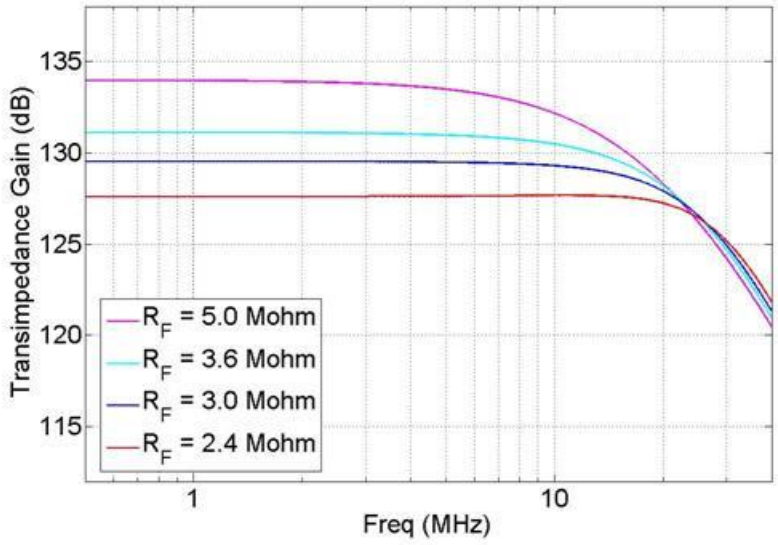


Figure 47. The transimpedance gain characterization with simulation.

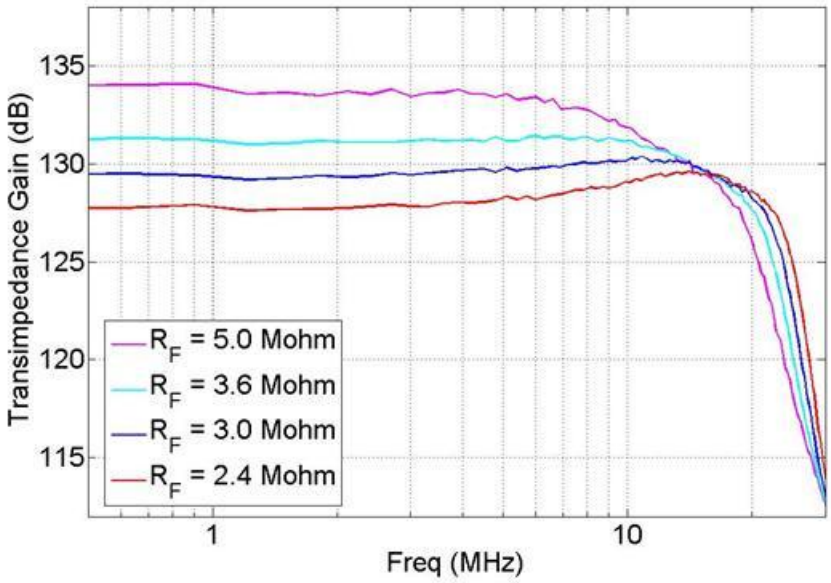


Figure 48. The transimpedance gain characterization with electrical measurement. Both measurement and simulation results demonstrate that the bandwidth is higher than 20 MHz for a 3-MΩ transimpedance gain.

In simulations, when the core amplifier has a 30 MHz open loop bandwidth, even a feedback capacitance as low as 5 fF significantly damps the circuit and reduces the closed-loop bandwidth. The measured results in Figure 48 agree well with the simulations where the only feedback capacitance comes from the very small 0.3 fF from the transistor model. Therefore it can be stated that even if there is an unexpected C_F due to parasitics, the measurement results suggest that it is much lower than 5 fF.

3.6.2. Noise Measurements

For noise measurement of the TIA, one of the outputs of the post processed IC in Figure 39 is connected to an Agilent 4395A in spectrum analyzer mode. No bias is applied to the receiver CMUT to only measure the front end electronics noise. The output

noise value of the TIA is obtained by dividing the measured output noise value by the buffer gain. Figure 49 plots the measured output voltage noise of the TIA for different values of V_{ctrl}. It should also be pointed out that the frequency shape of the output voltage noise agrees with the theoretical shape shown in Figure 32. The measured plots clearly depict the change in the TIA output noise spectrum with changing feedback resistance. At higher frequencies the TIA output noise starts to roll off, which is governed by the TIA transfer function. It should be noted that noise measurements at the output of TIA can also be used as an indirect way of extracting the gain and bandwidth information. For low frequencies output noise is dominated by the feedback resistance noise which is equivalent to $\sqrt{4kTR_F}$. Therefore, each noise level at low frequencies corresponds to the thermal noise of the respective tuned R_F value. Therefore gain information of the transimpedance amplifier can be extracted from the flat region of the output noise spectrum. In addition, for a critically damped TIA, the output noise peaks and starts to roll of around the 3dB frequency of the closed loop transfer function. Therefore, the bandwidth of the transfer function of the TIA can be estimated from the output noise spectrum. It can be seen that for the R_F = 3 MΩ case, the output noise does not start to roll off until 20 MHz. This observation supports the TIA gain measurements demonstrating a 3-MΩ gain with a bandwidth higher than 20 MHz.

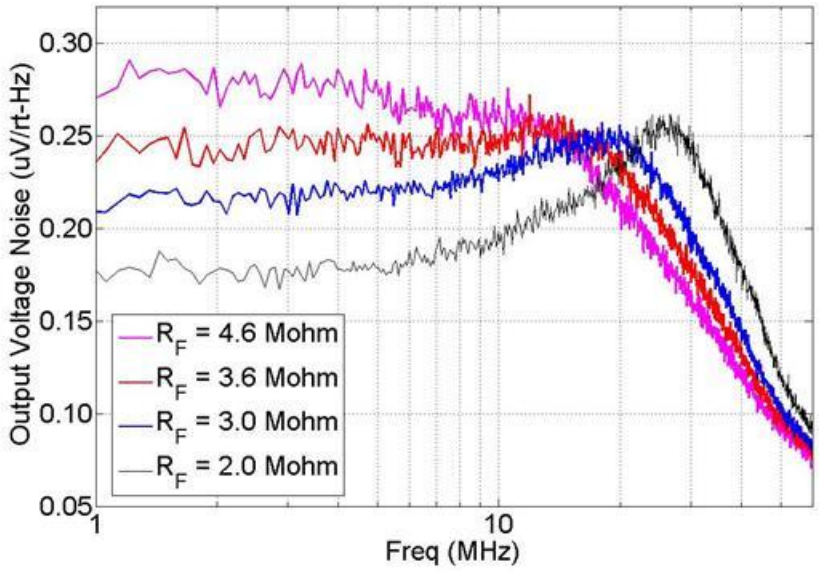


Figure 49. The output voltage noise of the TIA that is monolithically integrated to a forward-looking CMUT element with various feedback resistances. For higher feedback resistances the output noise starts to roll off at smaller frequencies as the TIA bandwidth reduces. The noise plot for the 3-MΩ R_F does not start to roll off until 20 MHz.

Figure 50 plots the measured, simulated and theoretically expected input-referred noise of the monolithically integrated TIA for a 3-MΩ feedback resistance. The measured input referred noise is obtained by dividing the measured output noise of the TIA by the TIA transfer function. The theoretical noise contribution of the feedback resistor and the core amplifier are shown separately along with the total calculated TIA noise. A 100-fF capacitance mimics the CMUT at the input of the amplifier in simulations. The theoretical core amplifier noise is calculated using the 1.1-nV/√Hz amplifier voltage noise and the 500-fF total input capacitance, which includes the CMUT capacitance and the amplifier input capacitances. The noise increase at higher frequencies is also visible from the plot. Thanks to the eliminated parasitic effects with monolithic integration and low voltage noise of the core amplifier, the core amplifier related noise does not exceed

the thermal noise of the feedback resistance until 20 MHz. It can be seen that the measured noise matches well with the total calculated and simulated noise values.

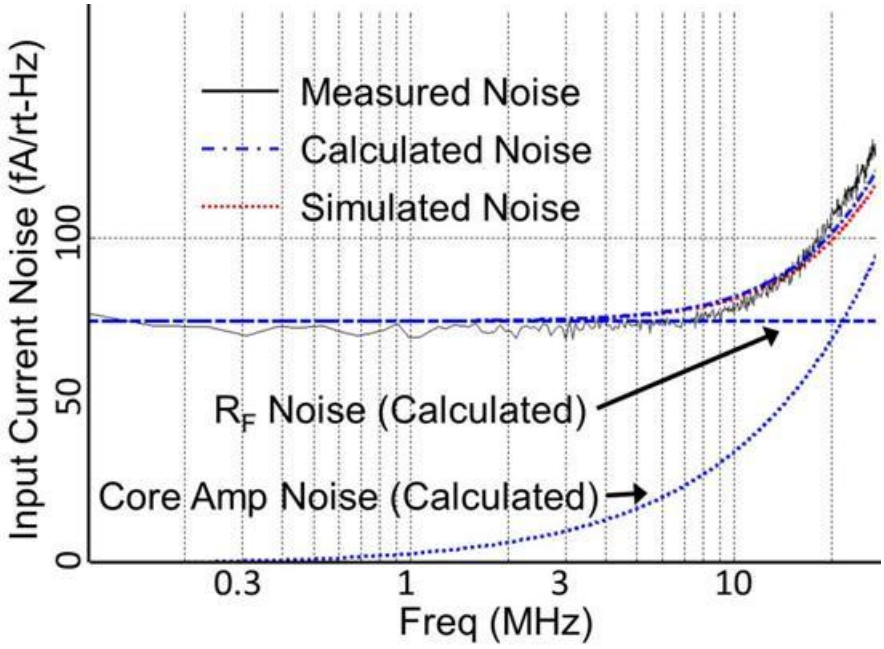


Figure 50**.** The measured and simulated input current noise of the TIA. The total theoretically calculated noise is also plotted along with the calculated feedback resistance noise and the calculated core amplifier noise. The measured 75-fA/√Hz feedback noise level at low frequencies is equivalent to the current noise of a 3-MΩ resistor.

Table 2. Summary of the key TIA and CMUT parameters

TIA PARAMETERS	
Technology	0.35 μm CMOS
Power Supply	3.3 V
TIA Area	40 μm x 110 μm
TIA Power Consumption	6.6 mW
TIA Gain	3 MΩ
TIA Bandwidth	20 MHz
TIA Input Current Noise Density (@ 15 MHz)	90 fA/√Hz
Buffer Power Consumption	3.3 mW
CMUT PARAMETERS	
Operation Frequency	10 – 20 MHz
Element Area	70 μm × 70 μm
R_{CMUT} (calculated)	1 MΩ
C_{CMUT} (calculated)	150 fF

3.6.3. Dynamic Range

The monolithically integrated 3-MΩ feedback TIA achieves an input referred noise current density performance of 90 fA/√Hz around 15 MHz. Total integrated TIA noise is 0.29 nA over 10 to 20 MHz CMUT band. To verify the spectrum analyzer noise measurements, a time domain noise measurement of the TIA is done using an oscilloscope and the output rms noise voltage at TIA output is measured as 1010 μV for 20 MHz bandwidth. This corresponds to a 225 nV/√Hz output voltage noise density assuming a uniform noise density over the 0 to 20 MHz range. When referred to input for a 3-MΩ gain, the input referred noise density is found as 75fA/√Hz. From the spectrum analyzer measurement, throughout the 0 to 20 MHz range the average current noise

density can be found to be around 83 fA√Hz. This value is close to the noise density value that the time domain measurement suggests.

The maximum input current that the amplifier can handle can be determined by the level where the amplifier gain changes by 1 dB from its small signal value. From simulations, the maximum peak to peak input current is found to be 20 nA. The 1 dB gain change point is also measured using the test setup shown in Figure 46. In the measurement, the maximum input current is found to be 37 nA. The difference between the simulated and the measured values is due to the typical process variation in the transistors when compared to the nominal model values in simulation.

The maximum dynamic range can be defined as [135]

$$DR_{MAX} = \frac{Maximum\,signal\,rms}{noise\ floor \times BW}. \tag{45}$$

Considering the 0.29-nA input noise floor and the maximum nominal (simulated) peak-to-peak input current of 20 nA, the preamplifier has 28-dB dynamic range. The dynamic range should be improved to at least 40 dB for satisfactory IVUS image performance. The major source of nonlinearity in the amplifier is the overdrive voltage of the feedback transistor that limits the maximum voltage swing at the TIA output. To implement the 3-MΩ resistance with the triode region NMOS with the aspect ratio of 0.4 μm/4 μm, the required $V_{CTRL} - V_{OUT} - V_T$ term in (40) is simulated to be around 44 mV. This overdrive voltage can be easily improved, while keeping the effective resistance the same, by using a longer feedback transistor. For instance, increasing the length of the transistor 4 times should also increase the maximum input current by 4 times and hence improve the dynamic range by 12 dB. One concern in increasing the feedback transistor length could be the capacitive loading of the transistor on the input node. The W/L =

0.4μm/4μm transistor in this design adds around a 5-fF capacitance from the input node to ground. For a 4 times longer transistor the added capacitance at input would be 20 fF which is negligibly small compared to the total capacitance at the input. To further improve the dynamic range, the high feedback resistance can be implemented with a T-network of resistors [135]. However, this approach degrades the noise performance [133] so this dynamic range improvement also comes in expense of the SNR. In addition, the resistors in the T network introduce parasitic feedback capacitance, which also limits the maximum feedback resistor that can be implemented. This also negatively affects the minimum input referred noise level.

3.6.4. Noise Measurements with CMUT in Liquid

To obtain measurements of the total system noise in immersion including the CMUT thermal-mechanical noise, a monolithically integrated IC was placed in a water tank. The output noise spectrum of the system at different CMUT bias voltages was measured (Figure 51). The output at 0 V represents the noise of the receiver electronics. As the CMUT bias is increased, the coupling coefficient and hence the CMUT noise contribution increases. Furthermore, as the CMUT bias is increased, the equivalent CMUT resistance decreases. For 0-V bias the effective resistance is infinite and for the highest CMUT bias R_{CMUT} is calculated to be close to 1 MΩ. In Figure 44, it was shown that the amplifier noise is independent of the CMUT resistance when the CMUT resistance is higher than 20 kΩ. Therefore changing the CMUT resistance does not modify the amplifier noise. On the other hand, with increasing bias, as the vacuum gap decreases, the CMUT capacitance increases to 150 fF from its 0 V bias value of 100 fF.

This increases the input capacitance term in (42) and results in a slight increase in the part of the amplifier noise that increases with frequency. However, the change in the CMUT capacitance is much smaller when compared to the total capacitance value at the input, which is around 500 fF. Therefore the increase in the amplifier noise with the increasing CMUT bias is expected to be very small. The frequency span of the CMUT noise is larger than the operation band of the device in immersion, which is from 10 MHz to 20 MHz. The source of the CMUT noise contribution from 5 MHz to 10 MHz is believed to be due to the acoustic crosstalk and the spurious waves in the substrate. Figure 51 clearly indicates that the CMUT thermal-mechanical noise dominates the output noise for 95V-dc bias, close to collapse voltage.

Noise figure (NF) describes the degradation of the SNR with the addition of the preamplifier. When all the amplifier noise sources are referred to input, the calculation of NF is given as

$$NF = 10 * \log\left(\frac{Noise\ Power\ of\ Amplifier + Noise\ Power\ of\ Transducer}{Noise\ Power\ of\ Transducer} \right) \quad (46)$$

With an ideal noiseless preamplifier the noise figure is 0 dB and the system SNR is limited by the thermal-mechanical noise of the transducer. As noise is added to the system by the preamplifier the noise figure increases.

The amplifier noise power, which is the noise level at 0 V bias in Figure 51, is around $(0.22\ \mu V/\sqrt{Hz})^2$. Between the 10-20 MHz range, the average total noise power at 95 V bias is around $(0.38\ \mu V/\sqrt{Hz})^2$. Therefore, the CMUT noise power can be extracted as $(0.38\ \mu V/\sqrt{Hz})^2 - (0.22\ \mu V/\sqrt{Hz})^2 = (0.31\ \mu V/\sqrt{Hz})^2$. Using the calculated values, the noise figure (NF) can be found as 1.8 dB using the noise figure calculation in (46).

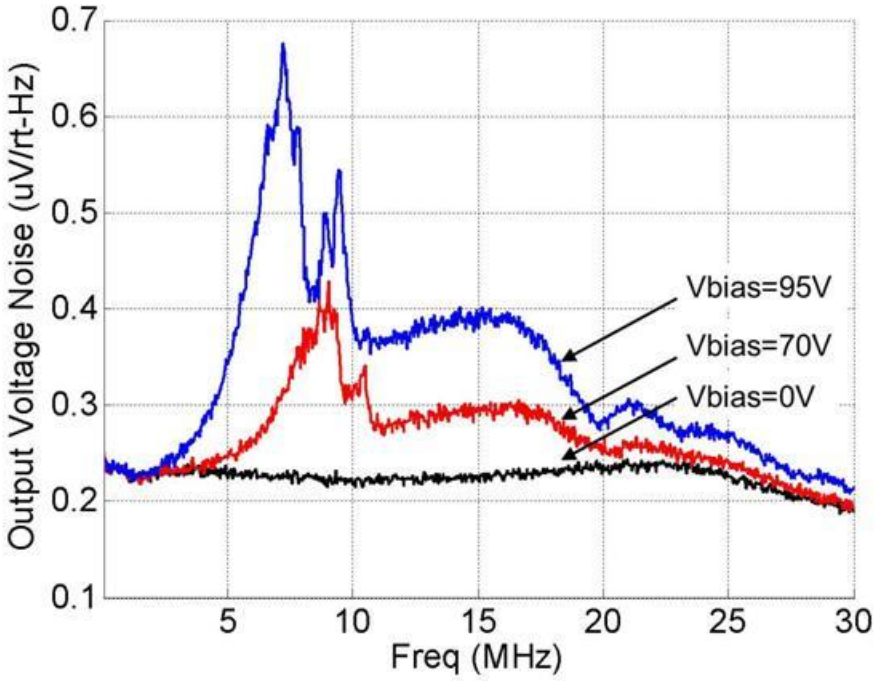


Figure 51. The system noise with 0V, 70V and 95V CMUT biases. When there is no dc bias, the noise is only due to the front-end electronics. As the DC bias is increased, the CMUT noise starts to dominate the system noise clearly demonstrating the transducer noise-limited receiver performance.

An important figure of merit for CMUT system performance is the input referred pressure noise. If one predicts the noise of an ideal CMUT, the minimum noise pressure due to the radiation impedance is $\sqrt{4kTR_{med}/S}$ where R_{med} is the real part of the radiation impedance in Rayls and S is the area of the transducer [114]. For the particular FL array element, this ideal CMUT noise can be calculated to be 2.3 mPa/√Hz where the radiation impedance of the CMUT element is considered equivalent to that of a circular piston with a 40 μm radius.

The noise equivalent pressure is experimentally found by using the measured output voltage noise in Figure 51 and a receive sensitivity measurement. A piezoelectric transducer is used as the acoustic source and the pressure at a particular distance is

measured with a hydrophone. Afterwards, the monolithically integrated IC-CMUT chip is placed at the same distance and the output voltage is measured. The receive sensitivity measurement based on the hydrophone measurements showed a 130 mV/kPa sensitivity at the TIA output when the CMUT is biased close to collapse. Using the result of the receive sensitivity; the measured output voltage noise is converted to an equivalent total input noise pressure. The noise equivalent pressure of the total system including the CMUT noise and the receiver circuitry noise is then found to be 3 mPa/√Hz at the center frequency. Based on this measured total noise equivalent pressure, the noise power ratio in Figure 51 suggests an amplifier noise of 1.8 mPa/√Hz and a CMUT noise of 2.4 mPa/√Hz. This measured CMUT noise is very close to the calculated and expected ideal case CMUT noise prediction of 2.3 mPa/√Hz, which considered the noise due to the radiation impedance and ignored the CMUT electrical and mechanical losses.

Table 3 compares the performance of front end receivers in literature that were designed for CMUT devices with the noted bandwidth and sizes. It can be seen that the TIA design in this work achieves the smallest noise figure. In [52], it is stated that the measured electrical noise does not change with the CMUT bias and concludes that the front end is preamplifier noise dominated. In [52], although the front-end is electronics noise limited, a smaller noise equivalent pressure is reported mainly due to a larger sized CMUT element. In addition, studies in [52, 111] use the same element as the receiver and transmitter and therefore requires protection circuitry to protect the low voltage receiver amplifiers from high voltage pulses. This protection circuitry introduces additional noise and degrades the receiver noise performance. One of the advantages of having separate rings for receive and transmit operation is that there is no necessity for a

TX-RX switch and a receiver protection circuitry, which is advantageous for low-noise detection.

Table 3. Performance comparison of receiver front-end designs for CMUT integration

	[111]	[52]	This work
CMUT Size	80 µm x 100 µm	250 µm x 250 µm	70 µm x 70 µm
TIA Bandwidth	>10 MHz	25 MHz	20 MHz
TIA Transimpedance	50 kΩ	215 kΩ	3 MΩ
Noise Equivalent Pressure	Not reported	0.9 mPa/√Hz	3 mPa/√Hz
Noise Figure	14 dB (simulated)	Amplifier noise dominated (measured)	1.8 dB (measured)

3.7. Volumetric Imaging Demonstration

The particular IC used for the imaging experiments is bigger in size compared to the IC in Figure 39 and is designed to integrate with a 1.6-mm diameter dual-ring array (Figure 52). This array is chosen for volumetric imaging experiments because it has a larger aperture and larger number of array elements than the other arrays concurrently fabricated. The used 1.6-mm diameter dual-ring FL-IVUS array consists of 64 receiver elements on the outer ring and 24 transmitters in the inner ring. The Rx elements contain 4 individual membranes and are approximately 70 µm x 70 µm. The Tx elements contain 8 individual membranes and are approximately 70 µm x 140 µm wide.

This IC also contains one transimpedance amplifier (TIA) for each receiver and four 16 x 1 multiplexers to route 4 receiver channels to the 4 output buffers. A conservative approach is used in the design of the transimpedance receive amplifier used in this IC. Instead of having a transistor in the feedback and a cascoded high gain bandwidth core amplifier as the ones used in the IC in Figure 39, a 20-kΩ poly-poly resistor is implemented in the feedback and the core amplifier is a non-cascoded common source stage.

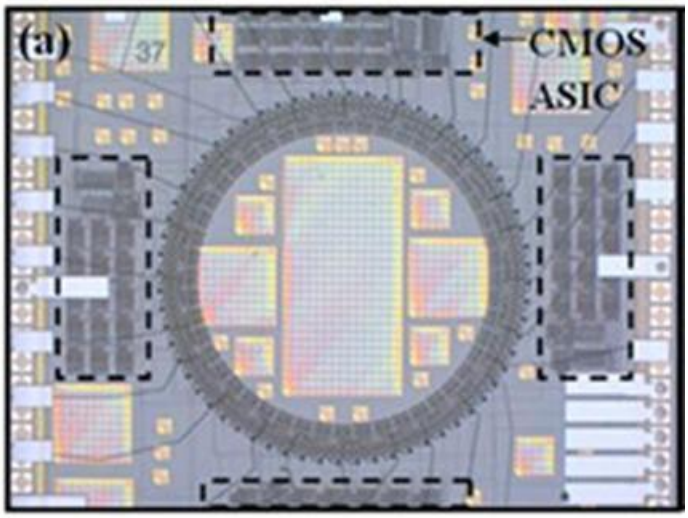


Figure 52. A fully fabricated CMUT on CMOS dual ring array with a 1.6-mm diameter for FL-IVUS applications.

To demonstrate that imaging can be performed with the FL-IVUS dual-ring arrays, a custom real-time data collection setup was constructed (Figure 53). The custom chip monolithically integrated with a forward-looking dual-ring CMUT array is first wirebonded to a ceramic dual inline package (DIP) and coated in 3 μm of Parylene C for electrical passivation in water. A small petri dish is glued directly on top of the array and then filled with water. A 60-mm diameter, 15-mm tall polystyrene Petri dish was

modified by milling a square opening in the base and then using epoxy to attach it to the ceramic DIP. This formed a cavity that could then be filled with water. Various targets can then be submerged in the water and positioned in front of the array for imaging. A custom pulser board is used to actuate the transmit elements. It can produce bipolar, high-voltage pulses up to 200 Vpp with bandwidths up to 50 MHz. A Xilinx Virtex 5 FPGA Evaluation Board is used to control the pulser board Tx element selection. It also multiplexes the amplified Rx signals to four parallel output lines which are subsequently digitized simultaneously using 4-bit, 250-MS/s digitizer cards. The digitizer cards can record up to 2.5 seconds of image data with a 100-MHz sampling rate.

The synthetic phased array method, which entails transmitting from one element at a time and then receiving the echoes from each individual Rx element, was used for image processing. The pulse-echo data for every Tx-Rx element pair was acquired for 20 μs (~1.5 cm imaging depth) without any time gain compensation or averaging. This results in a real time data acquisition rate of 130 frames/s considering 1536 Tx-Rx combinations and 4 parallel receive channels. Delay and sum algorithms are then used to create a volumetric image from the combination of all pulse echo data sets.

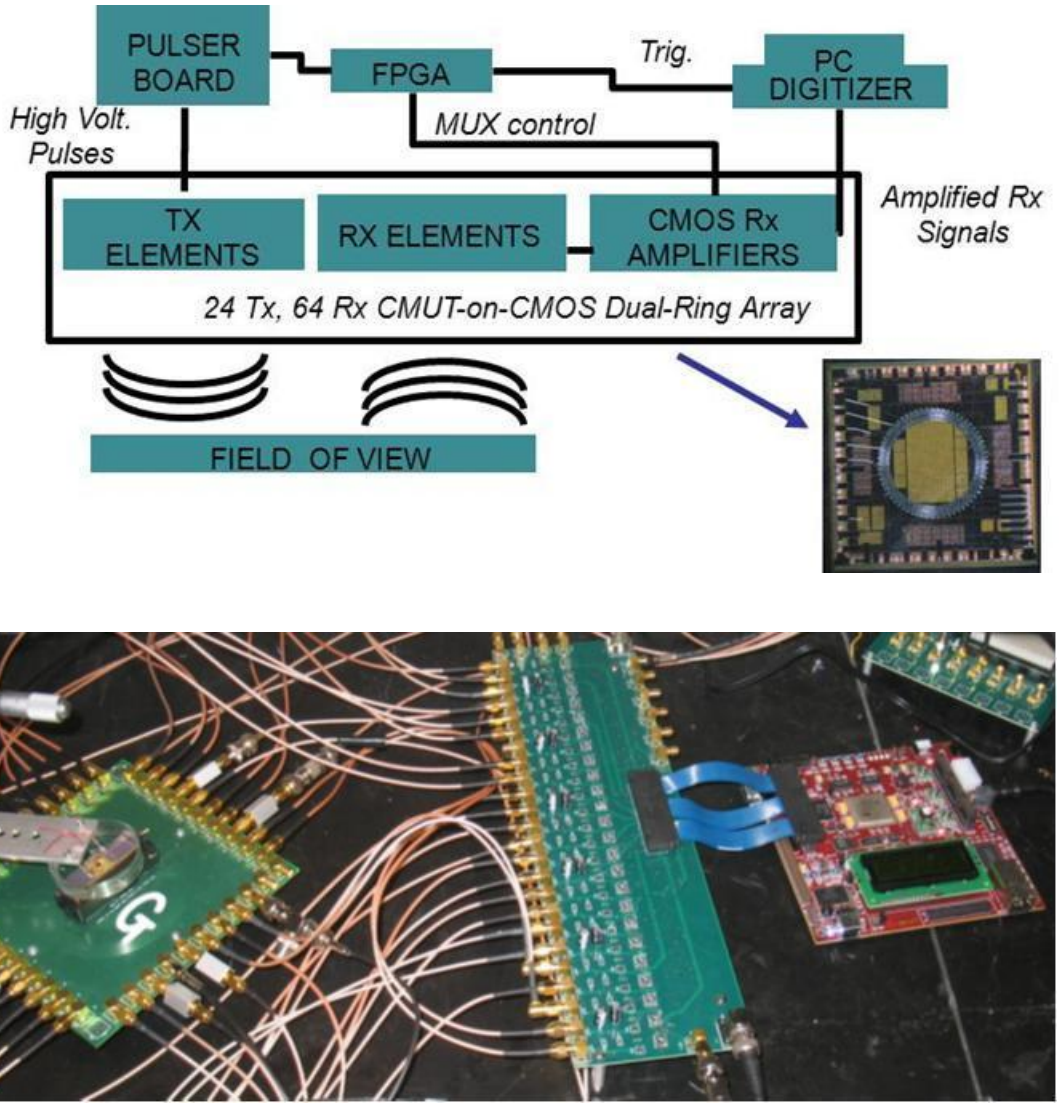


Figure 53. (Top) Block diagram of the real-time imaging setup for volumetric image data collection. (Bottom) Picture of the volumetric imaging setup

For imaging, a target consisting of a 100-µm copper wire embedded in a phantom with tissue-like scattering properties was constructed (part of Cone Instruments VP-1 Single Vessel Training Phantom, Model Ves-1K). This target was placed into the water filled Petri dish and positioned directly above the imaging array. The Rx elements were biased at 78 V. The Tx elements were biased at 70 V and then a 60-ns, 140-V_{pp} bipolar pulse was applied to them. The received echoes were then digitized and recorded for

subsequent image processing. Pulse echo data was acquired and a 4 x 4 x 9 mm^3 volumetric image with a 15-dB dynamic range was created using synthetic phased array image reconstruction. Two cross-sectional views and one isometric view of this image are shown in Figure 54. The water-phantom interface, the embedded wire, and a strong echo from the scattering phantom-air interface located 8 mm above the array are easily distinguished in the image. This image would not typically be used for diagnostic purposes with the strong echo from the phantom-air interface, but it demonstrates the functionality of the system. Using our custom test setup, we also imaged a target consisting of four 150-µm wires (Figure 55). A 2x2x6-mm reconstructed image of the 4 wire target is shown in Figure 55 with a 15-dB dynamic range, and a starting height of 2 mm above the surface of the array. These initial results obtained with over 100 frames/s data acquisition rate clearly demonstrate the capability of the CMUT-on-CMOS approach for single chip FL-IVUS imaging arrays especially for CTO type applications.

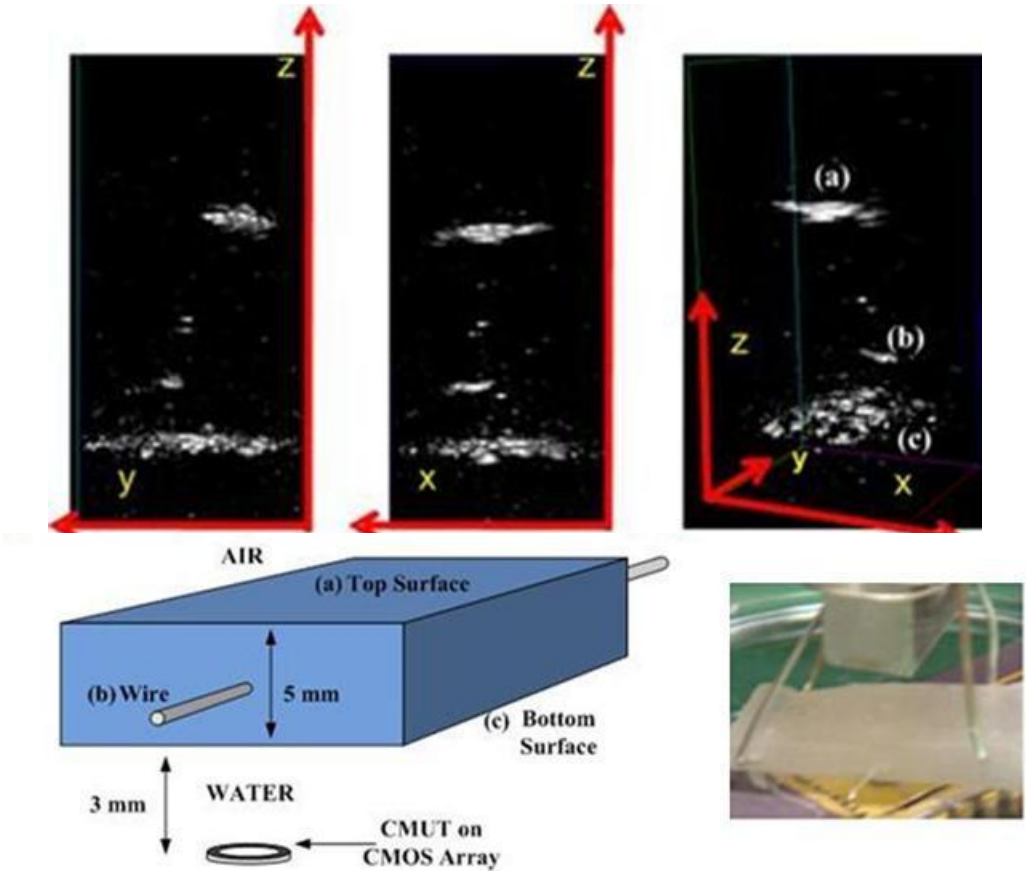


Figure 54. (Top) 2 cross-sectional views and a single isometric view from the 4 x 4 x 9 mm^3 volumetric image of the tissue-like phantom target with embedded 100 µm wire. The water-phantom interface, embedded wire, and upper phantom-air interface can all be clearly distinguished. (Bottom) Illustration and picture of the imaging setup consisting of the phantom target placed directly above the CMUT-on-CMOS dual-ring array.

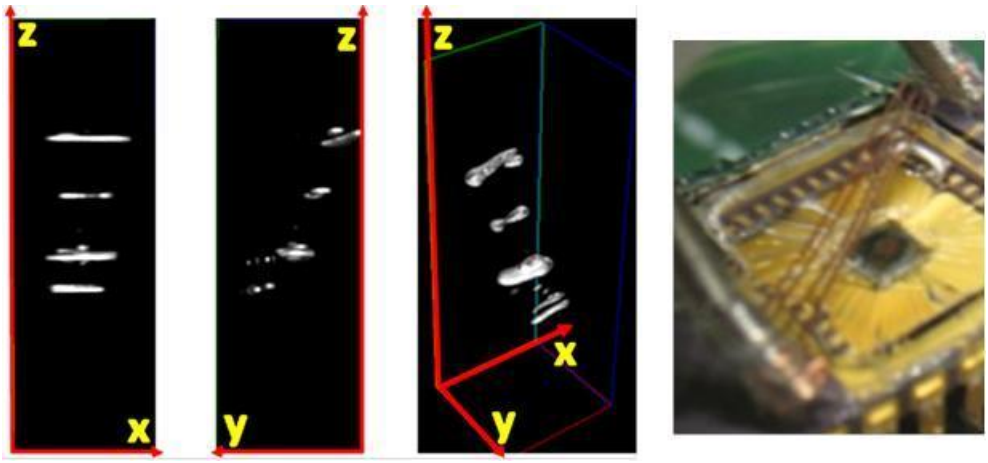


Figure 55. Side, front, and isometric views of a 2mm x 2mm x 6mm volumetric image of a 4-wire target along with the test setup.

3.8. Conclusion

The monolithic CMUT-CMOS integration offers improved overall sensor performance, smaller size and easier packaging with a small number of external connections. We discussed the design and implementation of a custom ASIC that is designed and fabricated in a 0.35 µm CMOS process for monolithic integration with a forward-looking CMUT array consisting of 70 µm x 70 µm elements. In the receiver design, the trade-offs between the gain, bandwidth, noise performance and the power consumption are discussed in detail. The transistor-feedback TIA design is shown to reduce the parasitic feedback capacitances and improve the low noise design. The successful monolithic integration of the CMUT array with the ASIC is demonstrated through a pulse-echo measurement. It is shown that the monolithic integration and the custom electronics designed for minimum noise enable transducer noise-dominated receiver performance with an input referred current noise density performance of 90 fA/√Hz and a 1.8-dB noise figure. Initial imaging experiments indicate the SNR obtained

with 100 frames/s data acquisition rate for over 1 cm imaging depth is sufficient to produce volumetric images of targets embedded in tissue-like phantoms in front of the array. With proper electrical interconnect and integration to catheters, the single chip, CMUT-on-CMOS approach appears to be a promising technology for challenging volumetric intravascular imaging applications.

CHAPTER 4

SINGLE-CHIP CMOS FRONT-END SYSTEM FOR FORWARD-LOOKING IVUS

4.1. Second CMOS Wafer Run

With the first wafer run, successful monolithic CMUT-on-CMOS integration for the demanding IVUS applications is demonstrated. Taking the developed core analysis and methods for the monolithic integration as the basis, a second 8-inch wafer in 0.35-μm two-poly, four-metal CMOS process including ICs with improved performance and additional capabilities is designed and fabricated (Figure 56-left). The ICs in this wafer are custom designed to monolithically interface with forward-looking and side-looking IVUS arrays with the sizes, the number of receive and transmit elements and the operation bandwidths given in Table 4.

It should be noted that the circuit design aspects for the ICs targeted for FL-ICE and FL-IVUS applications are very similar. However, the IC design for the FL-IVUS application is more challenging compared to the FL-ICE application in terms of the available area. Therefore, in this chapter, the design of the ICs for the implementation of single-chip forward-looking miniaturized systems is discussed mostly focusing on the FL-IVUS imaging application. The custom designed ICs for integration with annular arrays for SL-IVUS are discussed in detail in Chapter 7.

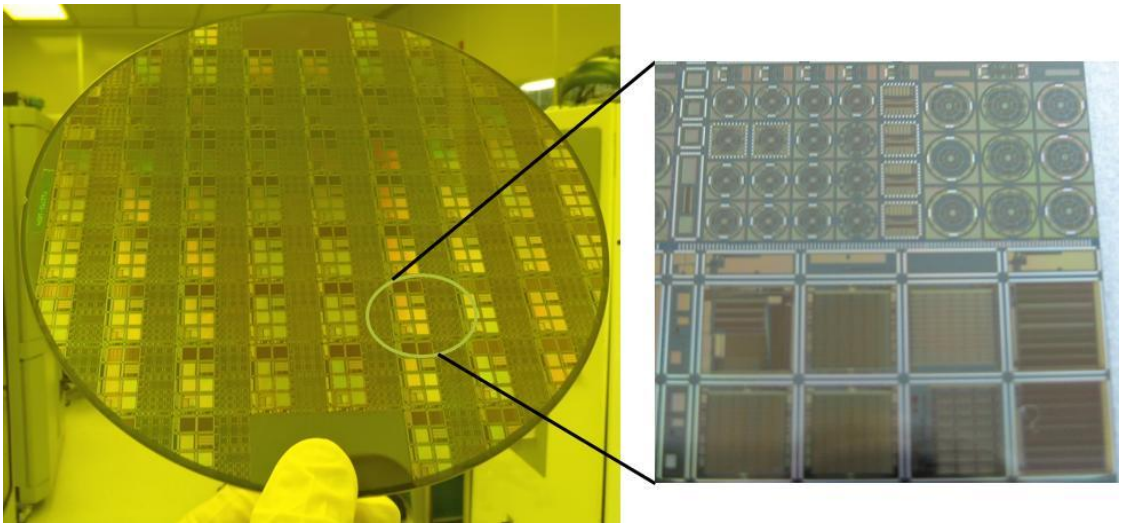


Figure 56. The picture of the second-generation 8-inch CMOS wafer fabricated in 0.35-μm CMOS.

Table 4. Array specifications

	FL-IVUS Array	FL-ICE Array	SL-IVUS Array I	SL-IVUS Array II
Array Structure	Dual-Ring	Dual-Ring	Annular	Annular
Catheter Tip Diameter	1.5 mm	2.1 mm	2 mm	1 mm
Array Size (Diameter)	1.4 mm	2.0 mm	1.6 mm	0.8 mm
Element Area	58 x 58 μm^2	80 x 80 μm^2	125000 μm^2	62000 μm^2
Number of Elements	56Tx-48Rx	64Tx-56Rx	8Tx – 8Rx	4Tx – 4Rx
Center Frequency	20 MHz	10 MHz	40 MHz	40 MHz

The first wafer run chip shown in Figure 39 designed for monolithic integration with the FL-IVUS CMUT array only included the receiver circuitry and did not incorporate the transmit electronics. This requires having the pulser chips on the side of

the assembly which necessitates many interconnects which is a challenge for a small-sized catheter. Considering the space and packaging constraints on the small catheter tip, integration of receive and transmit electronics and transducer array elements on a single chip is critical for successful implementation of a highly flexible forward-looking imaging catheter (Figure 57). Single-chip integration reduces the interconnect complexity significantly, and enables ultimate miniaturization of IVUS arrays. Therefore, in the second generation chip designs for FL-IVUS and FL-ICE applications, high voltage pulsers, low noise receiver electronics dedicated to each array element, multiplexers, buffers to drive the cables and the digital circuitry to synchronize the transmit and receive events are fit into a single IC to implement the complete front-end system in a single chip. These designs form a critical step to move into the system development phase for the implementation of the final forward-looking imaging catheters.

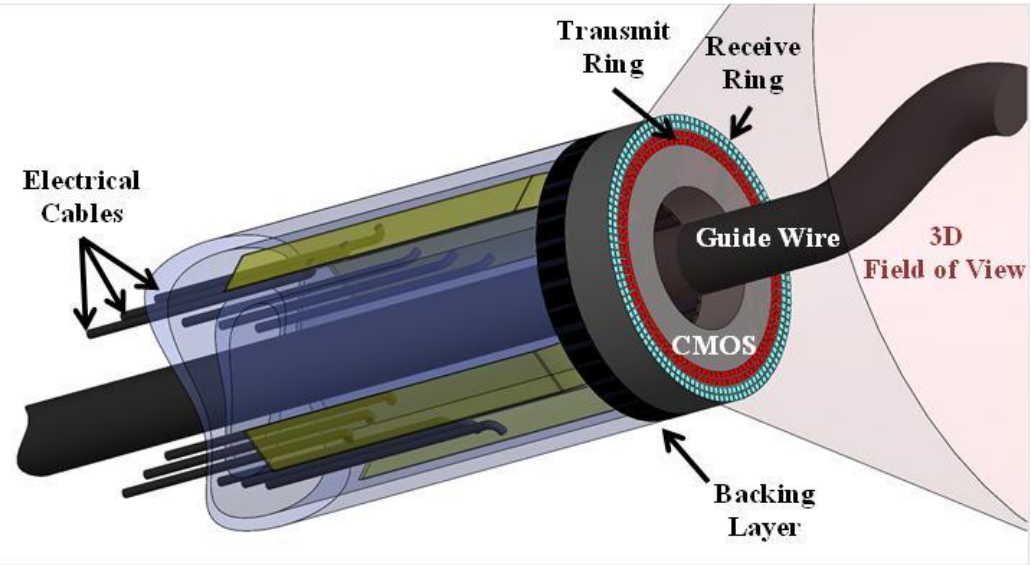


Figure 57. Conceptual drawing of a single-chip fully-integrated FL-IVUS imaging catheter based on a dual-ring CMUT array monolithically integrated with the complete front-end CMOS IC.

In the first wafer run the receiver electronics were designed without the strict layout limitation. However, in the new designs since the transmitter and digital control circuitry are to be fitted in the same IC with the receiver electronics the layout area is very limited especially for the 1.4-mm diameter FL-IVUS array. Therefore, in this second wafer run, the receive amplifier designs are reworked to reduce the layout area to fit the transmitter and receiver circuitry under a tight donut shape with an outer radius of 1.5 mm.

As discussed earlier, the power requirement is very tight for a dense single-chip IVUS imaging system, where there is not much space for the generated heat to dissipate. For instance the average power budget for solid-state IVUS catheters is set to 100 mW [44] to make sure that the temperature of the catheter does not increase to damaging levels when the catheter is powered and allowed to dry. The first generation FL-IVUS receiver chip was designed without a strict power limitation and 32 TIA elements consumed a total of 64 mA of current from a 3.3 V supply, which exceeds the 100 mW power budget [44]. Similarly, other studies using CMUT-based arrays and flip-chip integrated electronics have not considered this power issue. In this work, the power requirement is addressed from two different angles. Primarily, to reduce the power consumption, a power on-off capability is added to the receive amplifier. The amplifiers that are not actively used are biased off by the digital logic and at any given time only four of the amplifiers that are connected to the outputs are kept active. Concurrently, to further reduce the chip power consumption, the receive amplifier designs are reworked to reduce their individual power consumption without significantly compromising their performance.

4.2. Single-Chip System for FL-IVUS

Figure 58 shows a micrograph of an IC that is designed and fabricated for monolithic integration with a 1.4-mm diameter 20-MHz center frequency FL-IVUS dual-ring array including 56 Tx and 48 Rx CMUT elements. The IC includes 56 pulsers capable of generating 25-V pulses and a low-noise receiver transimpedance amplifier for each of the 48 CMUT array elements. The chip also includes buffers and a digital control circuitry that is designed to synchronize transmitting and receiving sequence during the data acquisition. All of the active circuitry fits into a size of 1.5-mm diameter silicon donut with a 430-μm gap left inside for a guide wire.

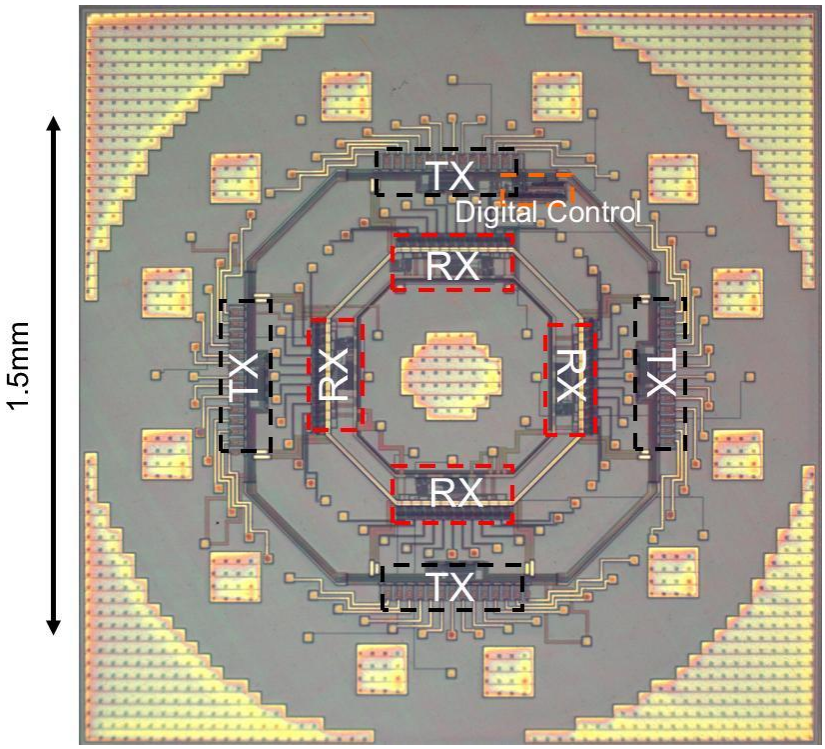


Figure 58. The micrograph of the IC designed for a 1.4-mm FL-IVUS dual-ring array with 56 Tx and 48 Rx elements. The IC includes 48 receive amplifiers, 56 pulser elements, corresponding multiplexers, digital control circuitry and buffers. All of the active circuitry fits into a size of 1.5-mm diameter donut area. Placement of receive and transmit electronics and the digital control circuitry are also shown in the picture.

The micrograph of the single chip system including the CMUT array monolithically fabricated on top of the CMOS IC is shown in Figure 59. Each CMUT array element consists of 4 membranes each with an electrode area of 20 μm x 20 μm. Silicon nitride thickness is 0.35 μm and vacuum gap is 0.16 μm. The CMUT array elements are designed with a 20 MHz center frequency and a 50% bandwidth, resulting in a frequency band between 15 MHz and 25 MHz. The CMUT element capacitance is calculated to be 90 fF.

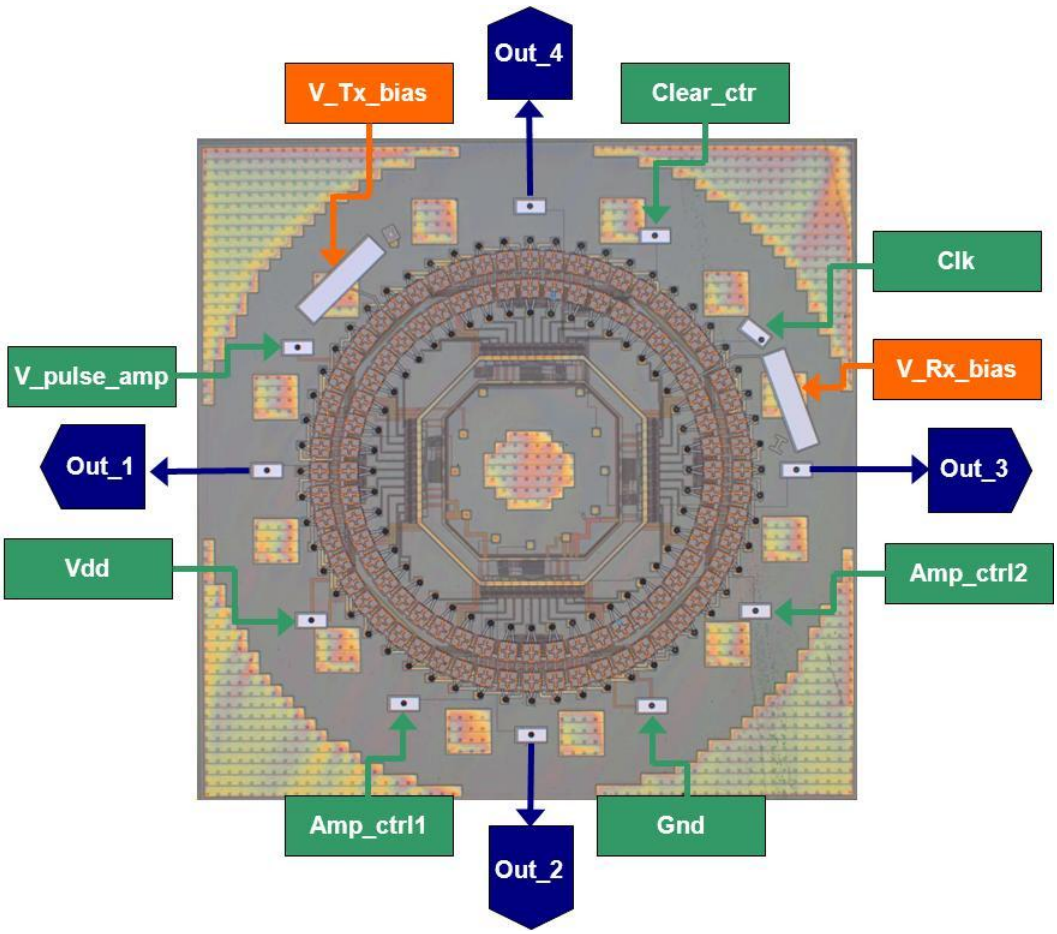


Figure 59. Picture of the IC shown in Figure 58 after CMUT fabrication. The external electrical connections to the imaging device are also shown.

The advantage of the fully-integrated single-chip system is clearly seen in Figure 59 which shows the external electrical connections to the imaging device. In this configuration, the data from 4 receive channels (*Out 1-4*) are collected in parallel. The *Clk* input has two functionalities. Its main function is to increment the counter in the digital control circuitry which synchronizes the chip. The *Clk* input is also used to generate the pulse trigger signal that is routed to the active pulser circuitry. *Clear_ctr* is the clear signal for the digital counter. *V_pulse_amp* voltage input controls the magnitude of the high voltage pulse. Two separate CMUT bias signals (*V_Rx_bias* and *V_Tx_bias*)

are provided for the separate receive and transmit CMUT rings. *Amp_ctrl1* and *Amp_ctrl2* are the two amplifier control voltages. These are Vbias and Vctrl for the resistor-feedback TIA design (shown in Figure 60) and Vbias and Vbias_gm for the capacitive-feedback amplifier (shown in Figure 65). The chip requires a total of 13 external connections with the vdd and gnd connections. Considering that the current 64-element SL-IVUS catheter requires more than 200 chip-to-chip and chip-to-transducer electrical interconnect bonds and only provides a single output channel, the enormous advantage of this novel single-chip approach can be better appreciated.

In this FL-IVUS application synthetic data acquisition is used and therefore no delay generation circuits are included on the IC. The reasons for not implementing a conventional phased array operation are twofold. The first reason is that to cover a 3D volume, an excessive number of steered ultrasound beams are required. This would increase the data acquisition time significantly which would increase the susceptibility to tissue-catheter motion artifact. The second reason is that having a beamforming circuitry would considerably increase the front-end complexity and it would be even more challenging to meet the stringent area and power requirements while trying to fit the phasing circuitry on this single IC.

For a dual-ring array the resolution does not depend on which ring is used as the transmitter or receiver. The choice between implementing a 56TX/48RX configuration or a 48TX/56RX configuration can be made based on area optimization. For instance, the inner ring with smaller number of elements can be assigned to the electronics block (receive amplifier or transmit pulser) that consume more area on the chip. However, in this design, the area of the implemented transmit pulser ended up being very similar to

the area of the designed receive amplifier. Therefore 56TX/48RX configuration is chosen arbitrarily.

With CMUT-on-CMOS integration, there is no need for wirebonding to the CMOS IC; therefore a pad structure (such as the one shown in Figure 39-left) consuming considerable chip real estate is not needed on the CMOS chip. Therefore, most of the ICs in the reticle are designed without any pad frame. However, it should be noted that, typically the pad structures also contain ESD protection circuitries and excluding the pad frame makes the chip more susceptible to ESD problems. Therefore, since at the time of the design the extent of the ESD considerations of excluding the pad frames were not clear, some of the ICs in the reticle are designed with a pad frame containing ESD protection circuitries. During prolonged experiments though the ICs without any pad frame remained to be functional, however, in the future designs to meet the industry standards, it might be required to include some ESD protection circuitry on the chips even though a pad structure is omitted.

The connections between the CMOS chip and the CMUT level are made through stacked metal layers that have a 25 x 25 μm area. In the particular IC shown in Figure 58, these connection areas consume their dedicated area in the layout. However, it is possible to eliminate the need for the layout area dedicated to the CMUT connections, by making the connections only using the highest metal (metal 4). This would allow having active circuitry directly underneath the CMUT-CMOS connection which is very advantageous for this very dense-area application.

Mainly two different low-noise receiver amplifier architectures are used for CMUT sensing in the FL-IVUS chips. One of the amplifier designs uses the resistor-

feedback TIA architecture and the second amplifier design uses capacitive-feedback architecture that are discussed in section 2.3. The performances of these two designs in terms of sensitivity, noise and dynamic range are investigated and compared in the following sections. It should be noted that for fair comparison of the two amplifier architectures, the amplifiers are designed with equal area and power consumption.

Table 5 shows the current consumption of the active preamplifiers and buffers separately along with the total chip power consumption. Note that the TIAs and the buffers are the main power consuming blocks and hence the power consumption of the pulser circuitry is neglected in the table. It can be seen that the average total power consumption of the chip is reduced to less than 20 mW by biasing off the unused receive amplifiers using the digital logic.

Table 5. Power consumption values for the sub-components of the IC designed for the FL-IVUS application

A single TIA	4 TIAs	4 Buffers	Total Current Consumption	Total Power Consumption
240 µA	~1 mA	4.8 mA	5.8 mA	19.2 mW

4.2.1. Improved Transistor-Feedback TIA Design

The transistor feedback TIA design and the sizings of the transistors implemented in the second wafer are shown in Figure 60. A source follower, which is not shown in the figure, is included between the TIA output and the output buffer. This source follower shifts the TIA output dc voltage (~0.7 V) to the preferred input dc voltage for the output buffer, which is around mid-rail (1.65 V).

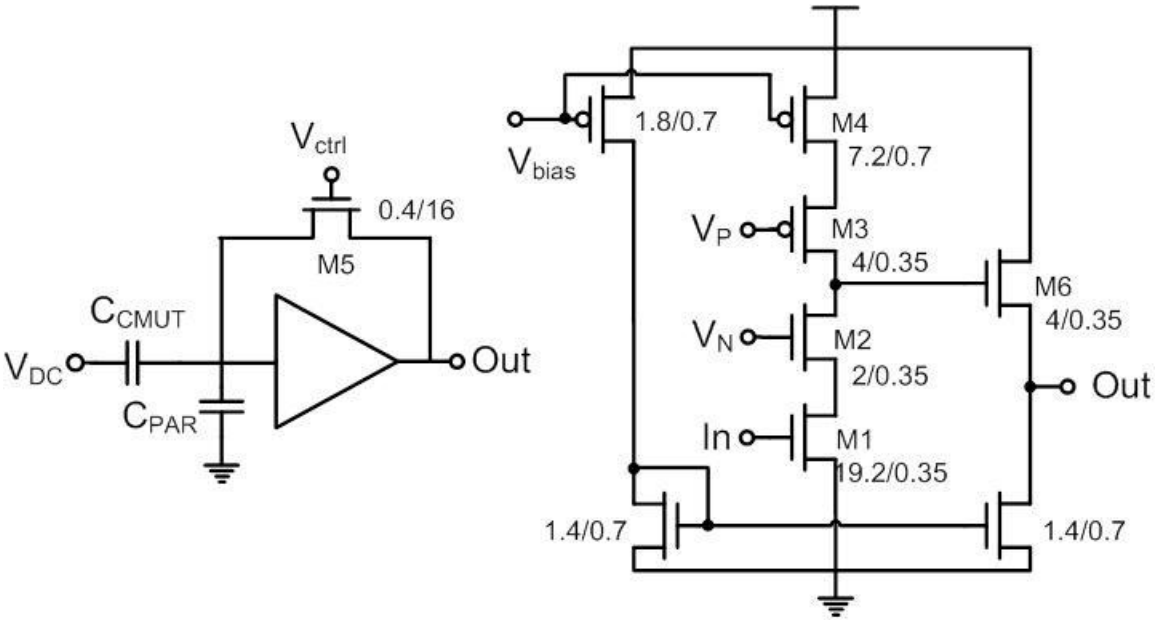


Figure 60. The resistor feedback TIA (left) and the full transistor implementation (right). Transistor dimensions are given in micrometers.

One important change in the design approach of this second-generation amplifier is related to the sizing of the input transistor. For the ease of the following discussion, the amplifier noise terms in the total input-referred current noise expression in (27) is repeated below.

$$\overline{i_{in,TIA}{}^2} \approx \omega^2 \left(C_{IN,AMP} + C_{PAR} + C_F + C_{CMUT}\right)^2 \frac{4kT\gamma}{g_m} + \frac{4kT}{R_F} \qquad (47)$$

In this expression the id^2/gm^2 term is substituted by $4kT\gamma/g_m$ where γ is the thermal excess noise factor of the technology. For MOS transistors with long channels this factor is given as 2/3 and for MOS transistors with sub-micron channel lengths it can be as high as 2. A study on the excess noise factor in 0.35 μm CMOS technology can be seen in [150]. From (47) it is apparent that increasing the width of the input MOS transistor size increases the g_m and reduces the voltage noise ($4kT\gamma/g_m$) of the TIA. On the other hand, increasing the width of the input MOS transistor results in a larger $C_{IN,AMP}$

which increases the noise. Therefore there is an optimum input transistor width that minimizes the core-amplifier related input-referred noise. To minimize the core-amplifier noise related term, the $(C_{IN,AMP} + C_{PAR} + C_F + C_{CMUT})^2/g_m$ term which is proportional to $(C_{IN,AMP} + C_{PAR} + C_F + C_{CMUT})^2/C_{IN,AMP}$ should be minimized. The minimum value is achieved when the amplifier input capacitance matches the sensor capacitance plus the parasitic caps at the input [151]:

$$C_{IN,AMP} = C_{PAR} + C_F + C_{CMUT} \tag{48}$$

However, it should be noted that in this derivation the dependence of the noise of the R_F term on $C_{IN,AMP}$ is not taken into account. The value of R_F is not independent of $C_{IN,AMP}$ due to the bandwidth tradeoff between the feedback resistance (R_F) and the total input capacitance. Another work, which also considered this effect of R_F noise, indicated that the optimum width is at a point where the input capacitance introduced by the core amplifier is smaller than the total of the CMUT capacitance and the interconnect parasitics [152]. Therefore in this design, compared to the initial design explained in section 3.4, the TIA input transistor size is reduced such that the input capacitance of the amplifier (~40 fF) is less than the capacitance of the FL-CMUT array element (90 fF). The reduced input capacitance (compared to the initial design) enables to have a lower g_m value while maintaining a core amplifier related noise (see the first term in (47)) that is similar to the initial design. This relaxes the required bias current level, which enabled to reduce the power consumption in this second-generation design. Furthermore, with reduced bias current, cascode and biasing transistors are designed with a smaller size (again compared to the initial design) which reduced the layout area of the design.

As mentioned earlier, to reduce the power consumption of the chip, at any given time only 4 of the total of 48 receive amplifiers are kept active. The bias currents of the unused amplifiers are cut off by switching the bias voltage to "Off" position through a digital switch. The digital control signals, which are connected to the receiver multiplexer selects (Rx<0:3>), are inserted to a de-multiplexing circuit that generates the control signals to shut down the unused amplifiers. Figure 61 shows a micrograph of a single TIA showing the power control switch (PCS) inside the TIA layout. It can be seen that the area for the power switching circuitry is much smaller and does not significantly affect the total area consumption of the amplifier.

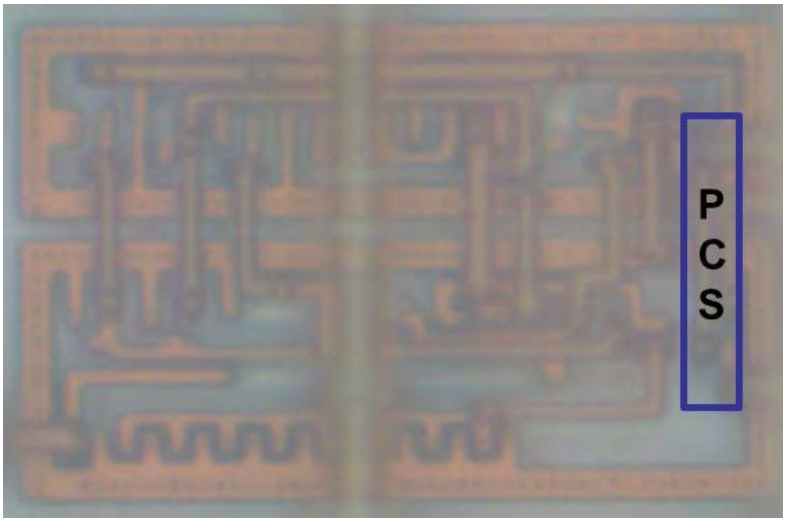


Figure 61. Micrograph of a single TIA and its power control switch (PCS). This demonstrates that switch circuitry that is used to switch the TIA power on or off consumes relatively much less area than the amplifier itself. The area consumption of a single TIA is 55 x 25 μm.

Figure 62 shows a simulated timing diagram depicting the operation flow for the power control. Transmit trigger signal is generated approximately 10 ns after the receiver is enabled. In this figure, the pulse repetition rate is 20 μs and the pulse width is 20 ns,

similar to normal operating conditions. A small sinusoidal signal is applied to the TIA input to show that the output is generated only when the power is turned on. When receive amplifier bias voltage is switched to “On” position it takes around 100 ns for the amplifier output to settle down to proper operation range. A peaking occurs during the transition of the amplifier output but it stays within the safe voltage limits of the transistor.

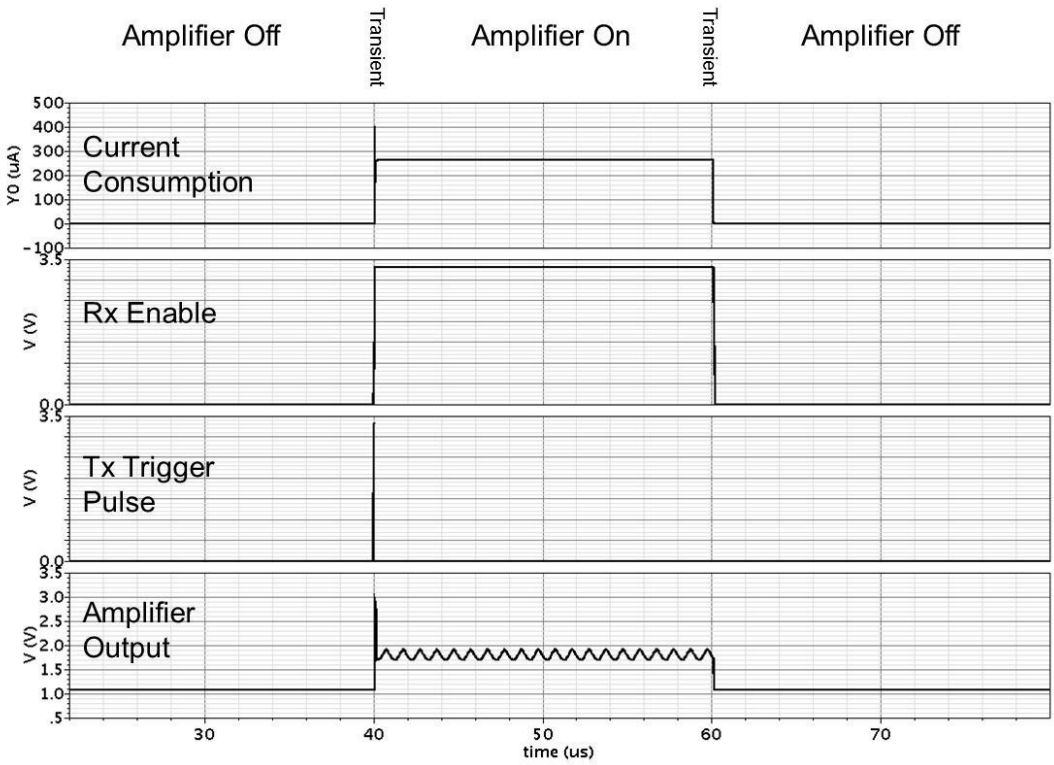


Figure 62**.** Circuit simulation results with a timing diagram that shows the Rx enable, which powers up the receiver circuitry, Tx trigger signal and the amplifier current consumption.

The transimpedance gain of the amplifier is measured at different feedback control values using the test setup shown in Figure 46 and the method discussed in section 3.6.1. The CMUT capacitance in the calculations is assumed to be 90 fF. The

measurement results of the amplifier demonstrated a gain of 630 kΩ with a 25 MHz bandwidth (Figure 63).

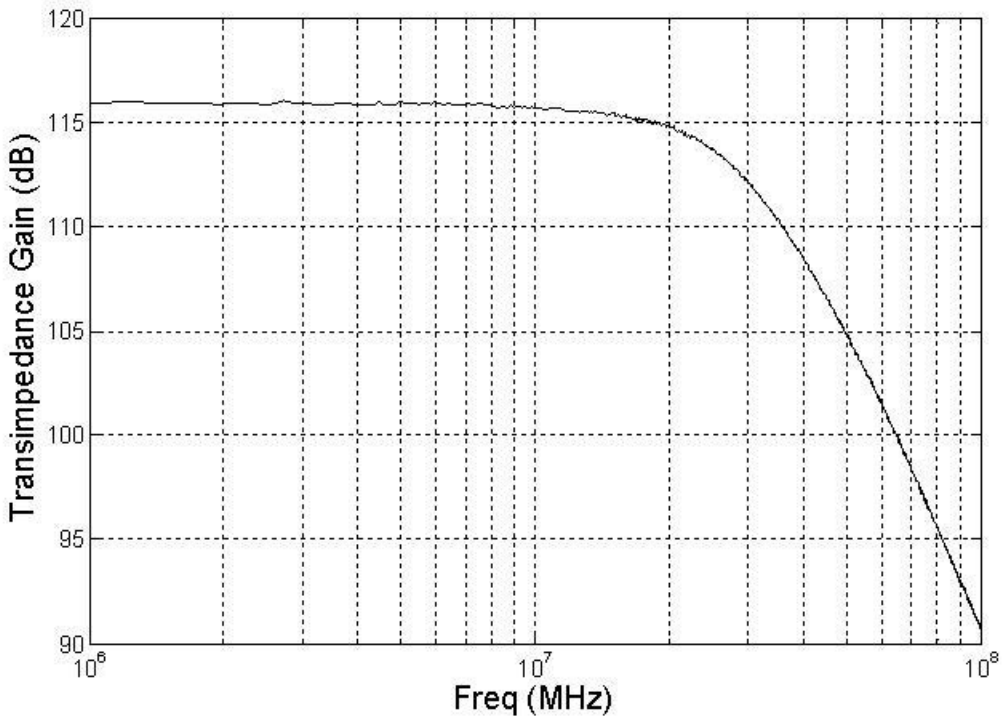


Figure 63. The measured transimpedance gain of the amplifier is 630-kΩ and the bandwidth is 25-MHz.

Figure 64 plots the measured total input-referred current noise of the amplifier. This figure is obtained by dividing the measured output noise by the gain of the amplifier. The measured input-referred current noise at 20-MHz center frequency is 220 fA/√Hz.

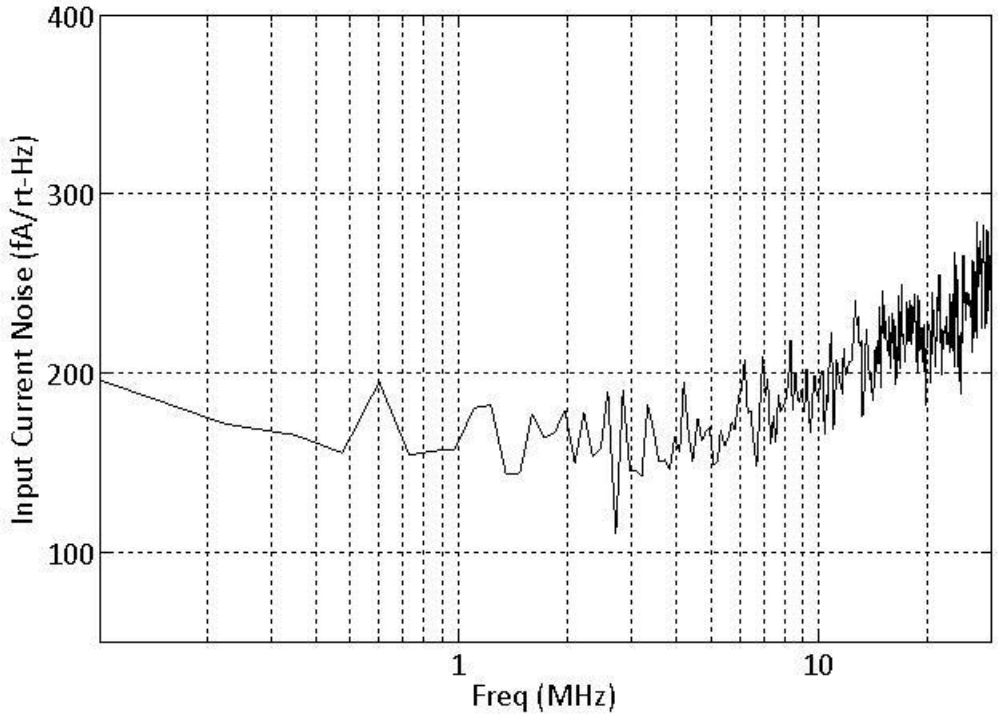


Figure 64. The input-referred current noise of the TIA that is monolithically integrated to a FL-CMUT element.

The dynamic range is found as 50 dB using the integrated noise value within the 15 to 25 MHz CMUT band. The dynamic range improvement compared to the initial design, which had 28-dB dynamic range, is partly achieved by reducing the W/L ratio of the feedback transistor by 4 times compared to the initial design. On top of that, the feedback gain is less in the second design which allows handling a higher input current.

This improved receiver TIA design consumes a 25 x 55 μm area which is significantly less than the area of the initial TIA design (40 x 110 μm) in the first wafer. In addition, this design consumes 240 μA current which is almost 1/8th of the initial design (2 mA) in the first wafer run.

4.2.2. Capacitive-Feedback TIA

Figure 65 shows the schematic of the designed capacitive-feedback TIA. The detailed gain, bandwidth and noise analysis of this architecture is presented in section 2.3.4.

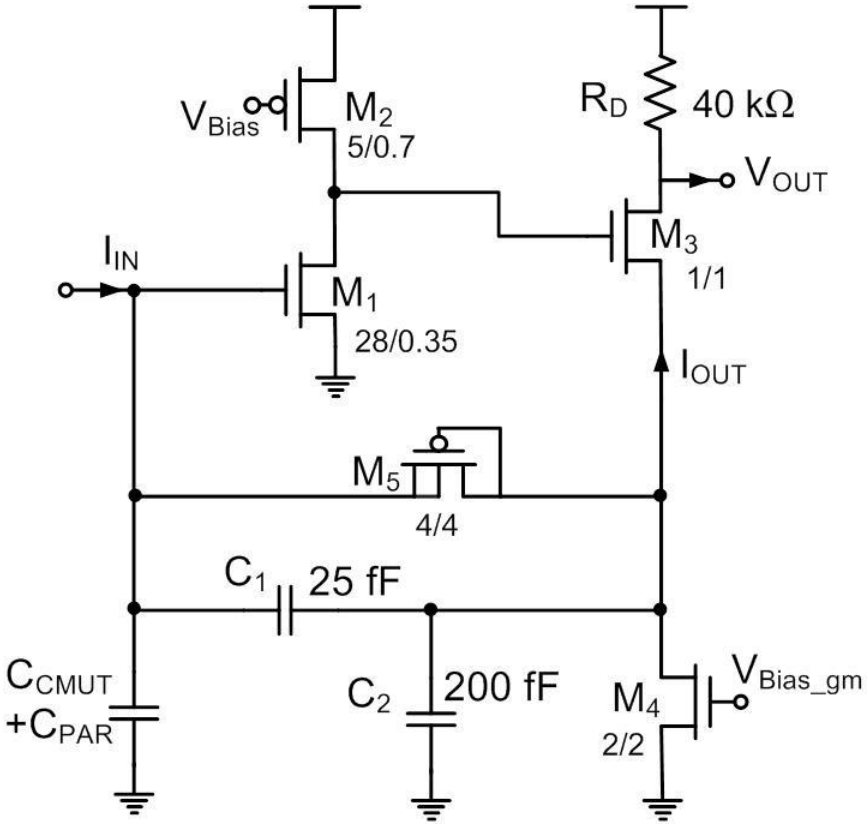


Figure 65. Schematic of the capacitive-feedback TIA. This TIA is designed to investigate its dynamic range and noise performance compared to the resistive-feedback TIA approach with a given area and power consumption for FL-IVUS application.

Note that the input dc node is floating when the feedback network only contains capacitances. Therefore a method to apply a dc bias to the input node is required. In this implementation, a MOS-bipolar device (M5) acting as a pseudo-resistor in parallel with the feedback capacitance is used [153]. It exhibits a very large resistance and sets the dc path to the floating input node.

The design consumes a 25 x 55 µm area and the simulated power consumption is 240 µA, which are the same as the area and power consumption of the resistive-feedback TIA design discussed in the previous section. Note that most of the current is consumed by the core amplifier (M1-M2). It is not explicitly shown in Figure 65 but there is a source follower that shifts the output dc point of the amplifier to around mid-rail for the connection to the buffer.

Figure 66 shows the gain measurement of the designed capacitive-feedback amplifier. This measurement is performed using the test setup shown in Figure 46 where the monolithically integrated CMUT capacitance (90 fF) is used for the gain testing. The measurement result demonstrates a transimpedance gain of 200 kΩ with a 40-MHz bandwidth.

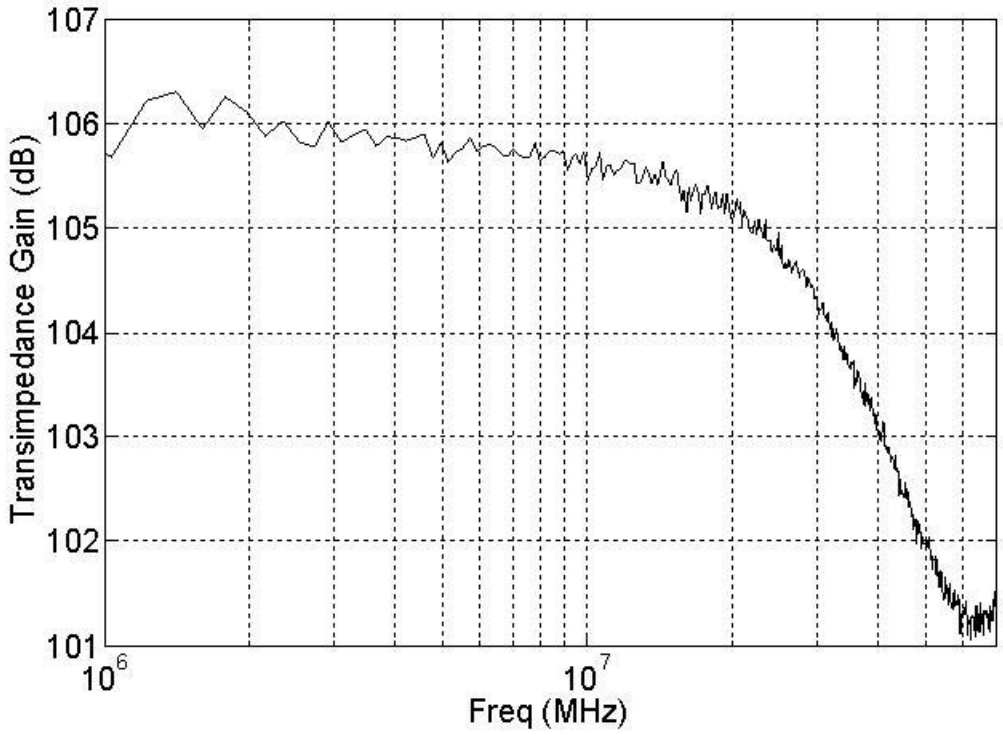


Figure 66. The measured transimpedance gain of the capacitive-feedback TIA shows a 200-kΩ gain and 40-MHz bandwidth.

Figure 67 shows the measured input-referred current noise of the TIA. In the current design the 3 dominant noise sources are R_D, M4 and the source follower (not shown in Figure 65). The measured spectral density of the noise at 20-MHz center frequency is 310 fA/√Hz. This value is higher than the 220-fA/√Hz input-referred current noise value of the transistor-feedback design. However, note that the input-referred current noise of this particular design is limited by the available area. The noise level could be significantly improved with a more relaxed area requirement, which would allow increasing the value of C_2 and R_D (see input referred noise equation in (39)). In the current design, the combination of C_1, C_2 and R_D consumes more than half of the total area already so for future designs there is not much room to increase the area of the capacitors without increasing the total area of the TIA. On the other hand, to save some area, in future designs, R_D, which is currently implemented with a poly-poly resistor, can be implemented with a transistor in triode region. This would allow increasing the value of R_D which would reduce the noise of the amplifier without requiring a larger area. In addition, in simulations, approximately $1/3^{rd}$ of the total input-referred noise is generated by the source follower circuit between the amplifier and the buffer. A higher R_D and a higher gain would also reduce the noise contribution of that source follower.

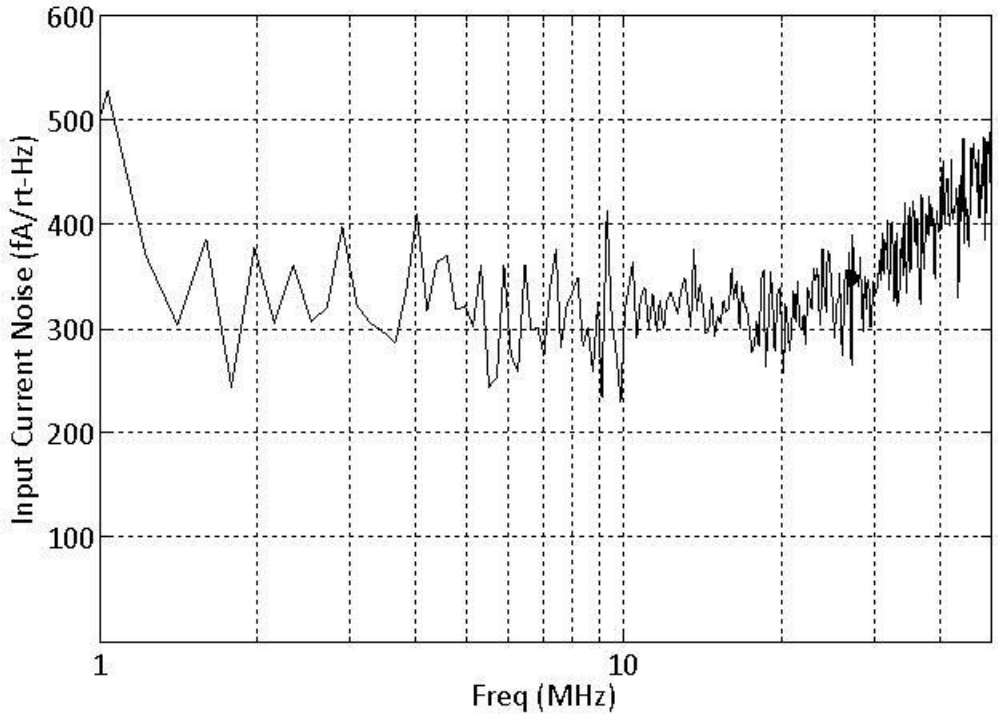


Figure 67. The measured input referred current noise of the capacitive-feedback TIA that is monolithically integrated to a forward-looking CMUT element.

The measured dynamic range of the amplifier is 50 dB. Table 6 puts together and compares the key performance values for the initial transistor feedback design in the first wafer and the two amplifier designs in the second wafer.

Table 6. Comparison of the designed receive amplifiers

	Transistor-Feedback TIA in Wafer I	Transistor-Feedback TIA in Wafer II	Capacitor-Feedback TIA in Wafer II
Input Referred Noise @ 15 MHz	90 fA/√Hz	220 fA/√Hz	310 fA/√Hz
Transimpedance Gain	3 MΩ	630 kΩ	200 kΩ
Bandwidth	20 MHz	25 MHz	40 MHz
Area	40 x 110 µm	25 x 55 µm	25 x 55 µm
Power Consumption	6.6 mW	0.8 mW	0.8 mW
Dynamic Range	28 dB	50 dB	50 dB

Before finishing this section, it should also be emphasized that if this capacitive-feedback TIA is interfaced with a CMUT element that had some current leakage then that current would get integrated over the feedback capacitance (C_1) over time, would distort the dc points and would prevent proper operation of this TIA. In that case, some way of periodically discharging the input node would be required [129]. However, a monolithically integrated IC that contained this capacitive-feedback TIA is used for imaging experiments and in those experiments the amplifier remained to be functional for prolonged experiments. This is important because it indicates that the leakage current of the fabricated CMUT elements is practically close to zero and also this TIA can be used to interface with CMUTs without a need for an additional circuitry that would periodically discharge the input node.

4.2.3. Digital Control

A digital control block is designed to synchronize the operation of the transmitter and receiver elements in the FL-IVUS array. It controls which of the amplifiers are the active receivers and also which pulser is the active transmitter. It runs on a single clock and manages the overall data collection process during the imaging. Figure 68 shows the top level view of the digital control circuitry. The FL-IVUS chip consists of 4 sub-blocks for receive and each receive sub-block contains 12 Rx channels (see Figure 58). In each receive sub-block, 12 Rx channels are multiplexed out through 4 multiplexer control bits, and a single receive channel is directed to its output at any given time. Since there are 4 receive sub-blocks, a total of 4 receive elements are routed to the 4 outputs of the IC simultaneously. Similarly, there are 4 sub-blocks for transmit (labeled as A, B, C, and D in Figure 68) and each transmit sub-block contains 14 Tx elements. Unlike the 4 simultaneously active receive channels, during the data collection, there is only a single active transmit element out of the total of 56 transmit elements.

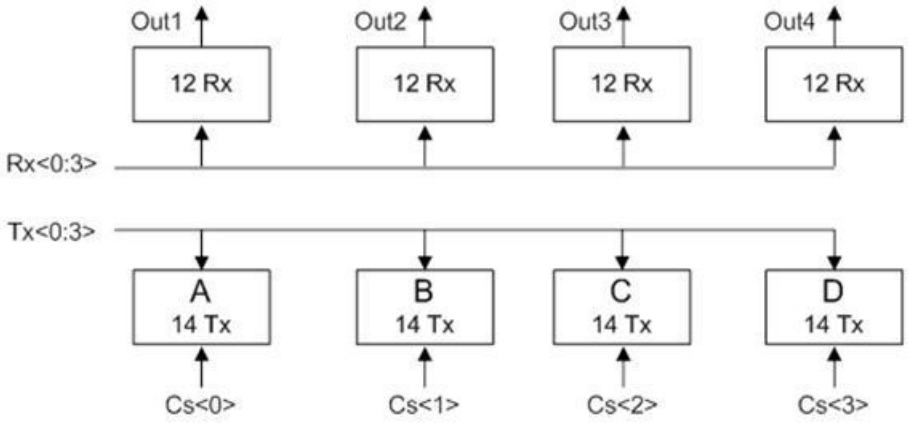


Figure 68. Top level view of the digital control for the dual-ring array.

The digital circuitry uses a Master Select block that provides the global control signals (Cs<0:3>, Tx<0:3>, and Rx<0:3>) that are routed to the sub-blocks (Figure 69). The master select includes a 10-bit counter. The 4 least significant counter bits (Rx<0:3>) are routed to the receive sub-blocks and control the 4 receive multiplexer selects to choose the active receive channel in each receive sub-block.

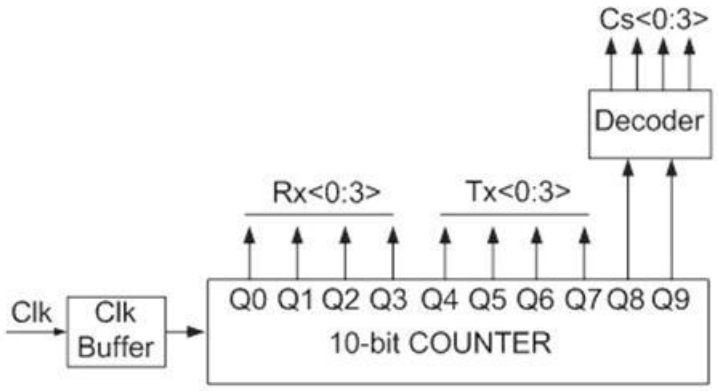


Figure 69. Master select circuitry

The two most significant bits of the 10-bit counter are inserted in a decoder that generates the Cs<0:3> signals. Tx<0:3> and Cs<0:3> signals are routed to the transmit sub-blocks. Each transmit sub-block contains a Local Select circuitry (Figure 70) that uses the Cs<0:3> and Tx<0:3> signals generated by the Master Select to control the transmit sequence. The 4 chip-select signals (Cs<0:3>) select between 4 different transmit sub-blocks and choose one of them as the active transmit sub-block. Tx<0:3> routes the pulse trigger signal to the active transmitter element in the selected active transmit sub-block.

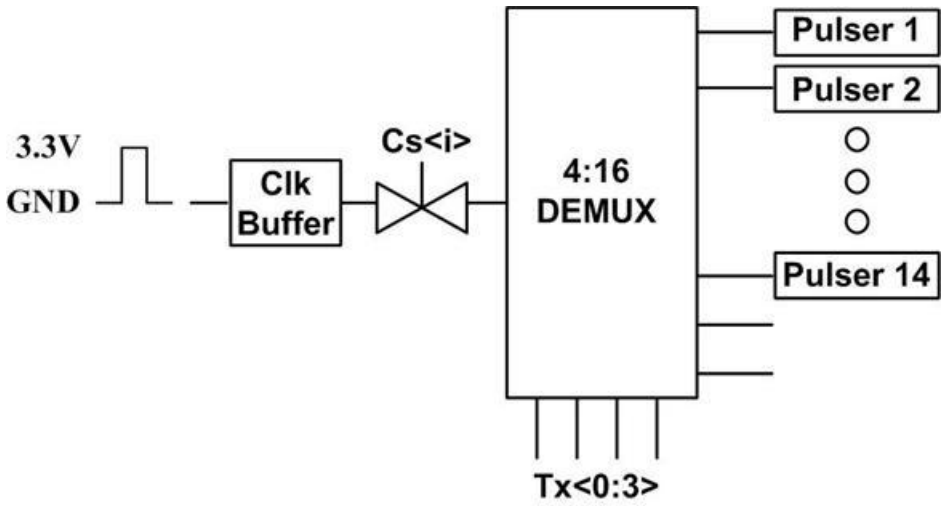


Figure 70. Local pulser select circuitry. Cs<i> allows the trigger pulse to propagate to the active pulser. Tx<0:3> selects the active pulser to be triggered by the external low voltage pulse. Note that the last two outputs of the de-multiplexers are not used because there are 14 pulsers in each transmit sub-block.

In summary the overall data collection sequence can be summarized as follows. First, Cs<0:3> assign an active transmit sub-block. Tx<0:3> choose a transmitter as the active transmitter in the selected active transmit sub-block. Active transmitter generates pulses for 16 times while Rx<0:3> cycle through all the receiver channels in each receive sub-block. Note that, since there are 12 receiver elements in each receive sub-block, the last 4 pulses (out of the set of 16 pulses) are not actively received. After the active pulser finishes transmitting by 16 times (in the meanwhile the receive data is collected from all 48 Rx channels for the selected transmitter), the digital control switches to a different pulsing element in the active transmit sub-block and the receive operation is repeated. Again note that since there are 14 transmitters in each transmit sub-block, the system generates a pulse for 14 times out of the 16 counts of Tx<0:3> and stays idle for the last two counts. After Tx<0:3> finishes counting up to 16 the system assigns a different transmit sub-block as the active sub-block and the whole operation is repeated. After all

the 56 transmit elements are switched around the array the data collection is completed. Thus, the data collection is synchronized through one clock and the whole imaging process gets finished in 1024 clock cycles.

It should be noted that the unselected demux outputs are actively pulled down to 0 V. This is critical as it prevents constant current flowing in the pulsers, which would be a major source of power consumption. Consequently, the pulser outputs sit at high voltage when there is no trigger pulse at the pulser inputs.

Typically, in mixed signal systems, which incorporate both digital and analog circuitries in a single chip, the digital and analog power supplies and gnd's are separated in the layout. This is desired because the switching noise of the digital circuitry may distort the analog circuitry. However, in this application, completely separating the digital and analog power supplies is not feasible because that would increase the number of electrical connections. In addition, the signal that is injected to the receiver circuitry from the switching of the pulser and the digital control circuitry is not a concern in practical pulse-echo operation. This is because for the first few hundred nanoseconds after the pulse, when the switching noise could be effective, the receiver is overloaded with the acoustic coupling in the surface and is not capable of processing any reflected signal anyways. Even though the digital switching noise might not be very problematic, as a first-order protection of the receiver amplifiers from the substrate noise, in the layout, the high voltage pulsers and the low noise receive electronics are surrounded by guard rings and isolated from each other.

4.2.4. High-Voltage Transistor and Pulser Design

In the 0.35-µm standard CMOS technology that the wafer is fabricated in the breakdown voltages of regular devices are less than 10 volts. To achieve higher pulse voltages within the limitations of the used technology, the maximum attainable breakdown voltage of an NMOS based on an "Extended Drain" approach (discussed in section 2.1.1) is studied.

Figure 71 shows the naming notation for the various lengths in an extended-drain high-voltage NMOS design. In this figure L is the channel length; D defines the overlap length of N-well in the channel; Lg is the gate overlap of field oxide; Ld is the distance between the poly layer and the drain and F defines the extension of N-well beyond the drain. It is important to investigate the effects of these parameters on the breakdown voltage to be able to maximize the achievable breakdown voltage.

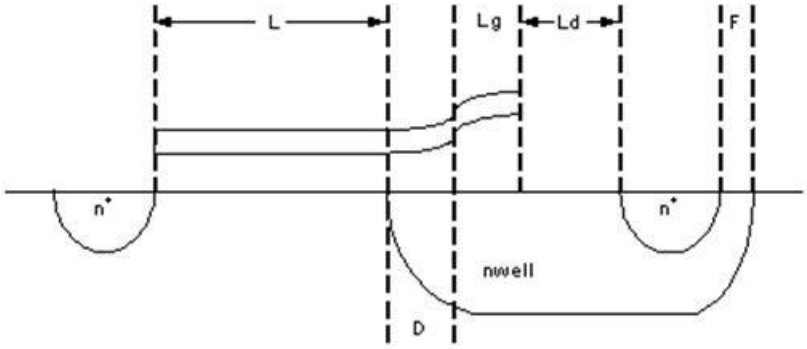


Figure 71. Extended drain NMOS

A through optimization of the breakdown voltage requires a deep knowledge of the technology parameters such as the doping concentrations. This information permits to perform complex physical simulations to characterize the effects of the design choices on the breakdown voltage [94, 154]. In our case, since detailed information of the process

parameters was not available, an experimental method which is similar to the work in [155] is chosen to evaluate the effects of each of the parameters shown in Figure 71. In the first wafer run 12 transistors with different lengths are laid out (Table 7). Note that because of the unconventional layout, the structures did not pass all the design rule check rules, which needed to be ignored. HV6 is taken as the base design and a single parameter is changed in every other design. This allows seeing the effect of a specific parameter to the breakdown voltage. In addition the electrical testing of these designs enables characterization of the devices (i.e. the on current) which are not modeled in the standard design kit.

Table 7. Sizes of the first set of extended-drain NMOS transistors in micrometers

	L	D	Lg	Ld	F	BV
HV1	**0.4**	0.4	1	6	2	36
HV2	**0.7**	0.4	1	6	2	34
HV3	**1**	0.4	1	6	2	34
HV4	**2**	0.4	1	6	2	34
HV5	**3**	0.4	1	6	2	34
HV6	**6**	0.4	1	6	2	35
HV7	6	**0.2**	1	6	2	35
HV8	6	**0.7**	1	6	2	32
HV9	6	0.4	**0.6**	6	2	33
HV10	6	0.4	**0.8**	6	2	34
HV11	6	0.4	1	**0.5**	2	34
HV12	6	0.4	1	**1**	2	35

In Table 7, for every design, the modified parameter that is under investigation is written in bold. For instance the designs from HV1 to HV6 are used to evaluate the effect

of L on the breakdown voltage. Similarly, HV6, HV7 and HV8 can be used to compare the effect of D. The measured breakdowns are non-destructive, meaning that the transistor remains to be operational when the voltage is reduced back to a lower level after the breakdown voltage is measured. Note that since the gate oxide thickness is the same as the standard low-voltage devices, the maximum gate-to-source voltages of these devices are still limited by the nominal supply voltage.

The minimum channel length of the standard devices in this technology is 0.35 µm and therefore the channel length on these high-voltage devices should not be less than 0.35 µm. Therefore the minimum channel length in these designs is chosen as 0.4 µm which is slightly higher than 0.35 µm. From the measured results in Table 7, it can be seen that all devices exhibit similar breakdown voltages independent of L. This indicates that the optimal gate length is less than or equal to 0.4 µm. Using a small channel length is advantageous in the pulser design for two reasons. The first reason is that a transistor with smaller channel length consumes less area in the layout. Secondly, with a reduced length the transistor switching gets faster. Therefore, the high voltage transmitter circuitry that is used on the single-chip ICs (i.e. Figure 58) in the second wafer run is based on HV1 which has the smallest length.

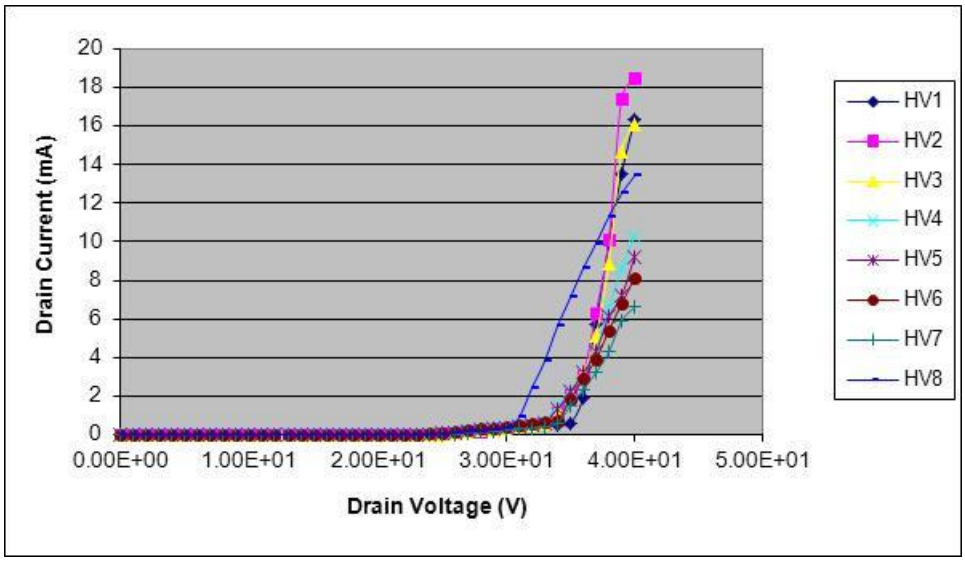
To investigate the effect of Ld while having a channel length of 0.4 µm, 3 more transistors are laid out in the second wafer run (Table 8). Out of all the tested 15 devices (including the ones in Table 7) the breakdown voltage seemed to be only impacted by D (see HV8) and did not show a strong dependence on the values of L, Lg, Ld and F. This indicates the Ld value can be reduced to 1 µm without any compromise on the breakdown voltage. This implies that in the next generation design the pulser can be

based on HV13 which uses an Ld value of 1 µm which is much smaller than the currently used Ld value of 6 µm. This result is important as it enables to reduce the layout area of the pulser elements. HV13 consumes 30 % less area compared to the high voltage transistor that is used in the current designs.

Table 8. Sizes of the second set of extended-drain NMOS transistors in micrometers

	L	D	Lg	Ld	F	BV
HV1	0.4	0.4	1	6	2	36
HV13	0.4	0.4	1	**1**	2	34
HV14	0.4	0.4	1	**3**	2	34
HV15	0.4	0.4	1	6	**1**	33

Figure 72 shows the drain sweeps of all of the 15 high-voltage devices that are shown in Table 7 and Table 8 while their gate voltage is kept at 0 V. Using these measurements, the noted breakdown voltages are determined based on the voltage where the drain current exceeds 1 mA.



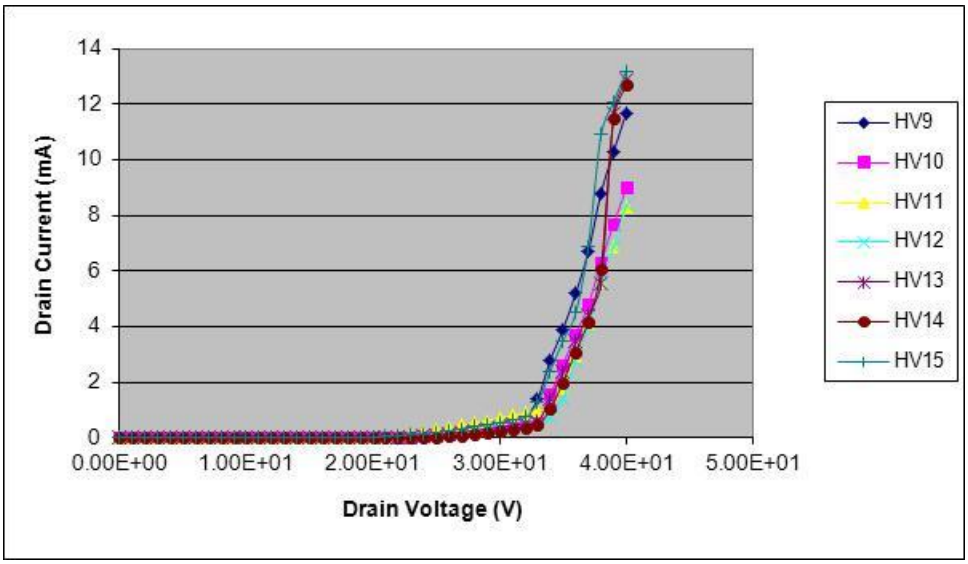


Figure 72. Drain voltage sweeps of the designed high-voltage NMOS transistors where the gate-to-source voltage is kept at 0 V. These measurements are used to find the breakdown voltages of the devices.

Figure 73 shows a drain voltage sweep of the HV15 design, which is very similar to the HV1 design used in the pulser elements. The only difference is the length F, which should not be affecting the on state current of the device. The width of the device is 36 µm which is also the width of high-voltage transistor used on the pulser design. The gate voltages are kept at 0 V and 3.3 V. Note that the measured I-V characteristics, especially

the on-resistance of the tested 15 high-voltage devices demonstrated minor differences. However, the aim was to find the transistor parameters that maximize the breakdown voltage with the minimum area consumption and therefore minimizing the on-resistance was not the primary objective.

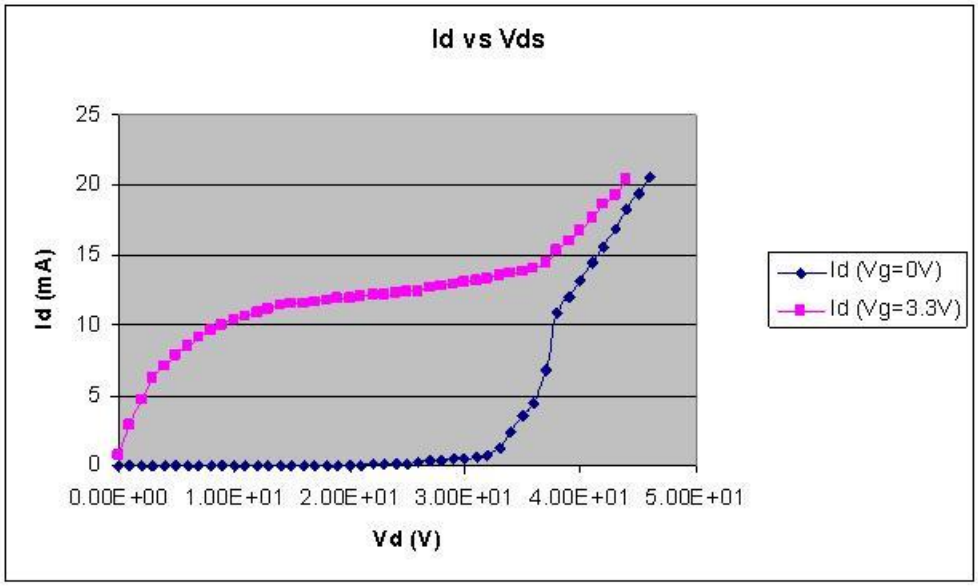


Figure 73. Drain voltage sweep measurements of the HV15 design with gate voltages at 0 V and 3.3 V.

Figure 74 shows the pulser circuit implemented on-chip that uses the HV1 NMOS design. A 3.3-V unipolar pulse is needed to trigger the pulser. The pulser converts the low-voltage input into a unipolar high-voltage pulse. The width of the output pulse is controlled by the width of the low voltage trigger pulse. To reduce the power consumption, the steady state voltage of the output pulser is at high voltage. Then when the input trigger pulse arrives the output switches from high to low.

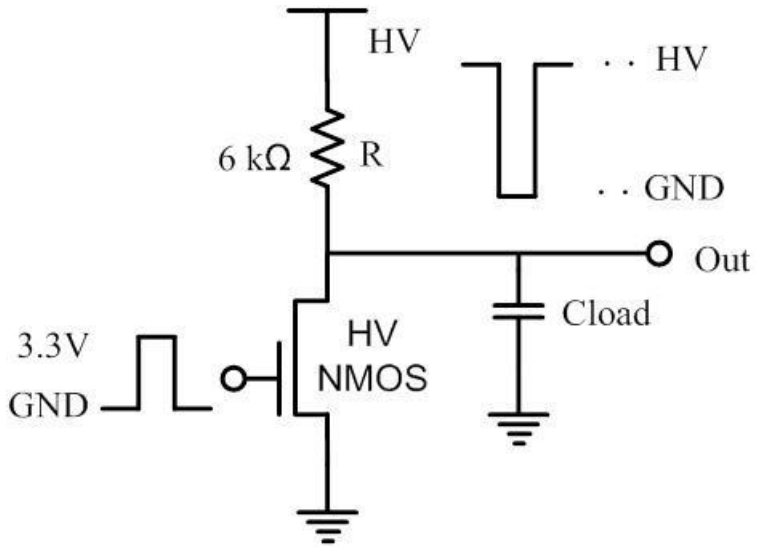


Figure 74. Pulser element

Figure 75 is a measurement result which shows a 25 V (2 V to 27 V) output pulse obtained from the pulser element. The trigger signal is a 100-kHz, 3.3-V square wave. Although each pulser individually can withstand drain voltages up to 35 V, during the imaging experiments, the pulsers in the IC are biased to a high voltage level of 27 V. The reason is that for instance with a 30 V drain bias voltage, when the pulser is not pulsing, each pulser has a leakage current on the order of 0.2 mA (Figure 72). When 56 of those are combined, the total leakage current of the entire pulser array becomes 11.2 mA which would be a significant source of power consumption from the 30-V supply. On the other hand, when the drain bias is reduced to 27 V, there is almost no leakage current and the pulsers do not consume notable power when they are off.

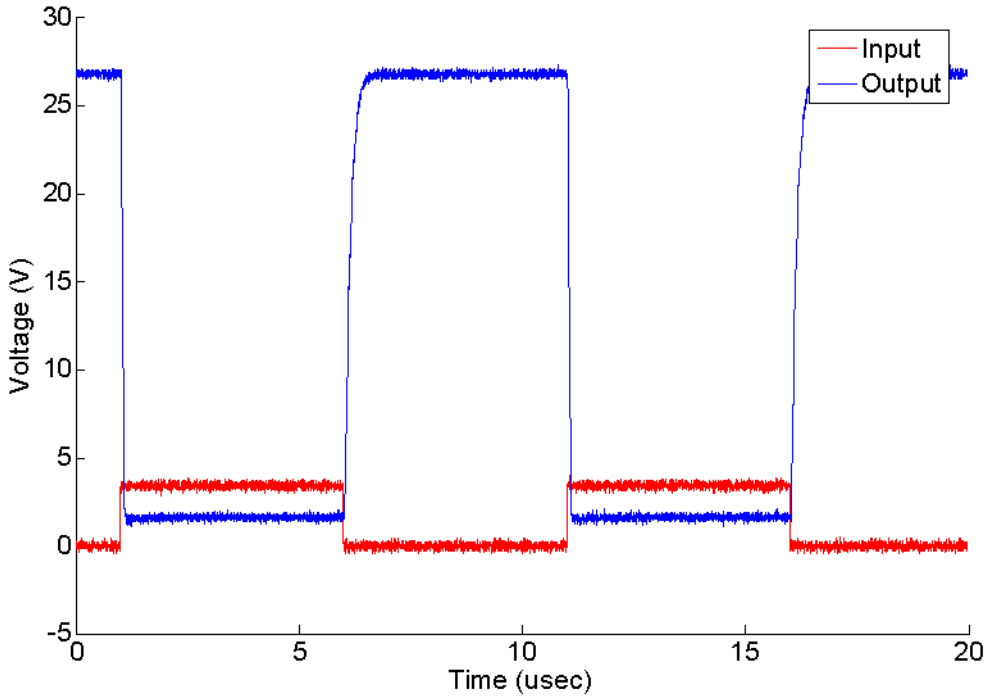


Figure 75. The measured output pulse which has a voltage swing of 25 V.

It is not possible to directly measure the speed of the output pulse because the capacitive loading of the cable and the scope used in the measurements give a pessimistic value for the speed. However, the speed for the CMUT loading case can be estimated using calculations. The measured rise time and fall time with the cable and scope capacitance loading is 255 ns and 60 ns respectively. From the rise time, which is equal to $2.2 \times R \times C_{load}$, and the known R value of 6 kΩ, the load capacitance (C_{load}) can be extracted to be 19.3 pF. For the CMUT-on-CMOS case, where the pulser is only loaded with the CMUT, the total capacitance loading at the pulse output includes the CMUT element capacitance, the capacitance of the high-voltage transistor and the parasitic capacitance of the resistor. Other interconnect parasitic capacitances are eliminated by monolithic integration. Since the used HV transistor is not a part of the design kit, it is

not possible to simulate the exact capacitive loading of the high-voltage transistor. On the other hand, even though the extended-drain design might exhibit slightly different capacitive behavior compared to a standard transistor, the capacitance of an equal-sized standard transistor can give a reasonable estimate for the capacitance of the high-voltage transistor. The simulated drain capacitance of a standard transistor with W/L = 36 μm/0.4 μm is 30 fF. The parasitic capacitance of the resistor used in the pulser can be roughly assumed to be 10 fF. Therefore, the total loading capacitance including the 90-fF CMUT capacitance becomes 130 fF. Both the rise and fall times improve proportionally with the reduced loading capacitance. Therefore, the rise and fall times for the CMUT loading case can be approximated as 1.5 ns and 0.5 ns respectively by projecting the rise and fall time values for the 19.3-pF loading case to the 130-fF loading capacitance of the monolithic CMUT connection. This calculation suggests that with this pulser design, it is possible to generate a pulse with a pulse width as narrow as 2.0 ns, which is more than sufficient to drive the 20-MHz center-frequency CMUT element.

From the output pulse measurement in Figure 75 it can be seen that the output voltage does not swing all the way down to 0 V, which is a drawback of using a resistive load. To obtain a low level that is closer to the gnd level, the resistor load can be replaced with a PMOS pull-up transistor. However, a high voltage PMOS transistor would consume much larger area compared to the resistor. On top of the PMOS pull-up transistor there would also be a need for a level shifter circuit (Figure 24) to drive the gate of the PMOS transistor which would require more devices and would increase the area. Since in this application, area is very limited, a simpler pulser circuitry approach including only a single high voltage transistor is chosen.

In the IC that is shown in Figure 59, to eliminate a dedicated external connection, the input pulse trigger signal is generated through the clk. The clk signal is internally delayed for around 10 ns and then routed to the pulser as the pulse trigger signal. The 10-ns delay is long enough for the switching transient to settle which ensures that the intended pulser to which the trigger signal is to be routed is properly selected. Since the clk is also used as the pulse trigger, its pulse width determines the width of the output pulse.

Alternatively, in the reticle there is an IC version where the pulse is not generated by the clock and provided externally to the IC. An advantage of providing the pulse trigger externally is that the counter clock can be run faster than the pulse trigger signal and some of the transmitter-receiver pairs can be skipped without pulsing. This allows collecting a reduced dataset, which allows having a faster data collection while maintaining the image quality [156].

Identifying the power consumption of individual functional blocks is important to understand the power bottle-neck of the system. In general, in B-mode imaging ultrasound systems, the receiver circuitry consumes more power than the transmitter circuitry. Although, transmitter circuitry generates high voltage pulses, the duration of the pulse is much smaller compared to the overall transmit/receive cycle duration and therefore the average transmitter power consumption is small. On the other hand, the receiver circuitry needs to be on for most of the imaging duration.

For this particular design, for the transmitter side, the power consumption can be estimated by considering the fact that each pulser discharges the load capacitance (C_{load} in

Figure 74) which is charged from a high-voltage source. The energy stored in the capacitor is given by the expression below.

$$E = \int VIdt = \int VC\frac{dv}{dt}dt = \int CVdv = \frac{CV^2}{2} \tag{49}$$

Thus, the dissipated power by the unipolar pulser is given by

$$P = \frac{CV^2 f}{2} \tag{50}$$

where V is the peak-to-peak output voltage and f is the pulse repetition frequency (PRF). Assuming a 25-V pulse amplitude, a 130-fF total load capacitance and a 20-µs repetition rate for a 1.5-cm imaging depth, the average power for each transmitter is only 2.0 µW. Comparing this value with the 0.8-mW power consumption of the receive amplifier indicates that in this application transmit elements consume much less power compared to the receive amplifiers. The power consumption of the logic circuitry is also relatively much lower as compared to the receive circuitry and can be ignored.

4.3. Catheter Integration

In the center of the ICs designed for the FL-IVUS application a 60-µm wide circular region around the metal fillers is left free of any metal traces or active CMOS circuitry (see Figure 59) to enable etching through the silicon substrate to create the opening for the guidewire. Similarly, a 60-µm wide circular region is also left empty for the outer perimeter etching to create the final donut shape suitable for placement on a tip of a circular catheter (Figure 57). A picture of the IC after the plasma etching for a donut shape is shown in Figure 76. The diameter of the gap at the center reserved for the guide-

wire is 430-µm. The outer radius of the donut shape shown in Figure 76 is 1.85 mm. However as discussed earlier, all the active circuitry and the CMUT array fits under a 1.5-mm diameter. The connection areas (for this particular chip they are bondpads) outside the diameter of the CMUT array are placed for initial testing of the IC with wirebonding and will be omitted in the final catheter implementation. In the final construction of the catheter, the necessary electrical connections for the chip will be made using the metal connection areas placed close to the center of the IC. Some of those electrical connection areas are circled in the magnified picture of a sub-section of the IC (Figure 76). In Figure 76, it can also be seen that there are some rectangular regions that are etched out within the donut region. These areas are reserved for through silicon vias (TSVs) which will be connected to the electrical connection areas in the center of the array. It should be noted that the capacitance and resistance loading specifications of the TSVs are not critical for this application because the only ac signals that will be connected to the TSVs are the buffered outputs. The TSVs will connect to the flex-tape on the backside of the IC. This discussed electrical interconnect scheme where interconnects are located within the confines of the diameter of the CMUT array enables a very tight integration of the single chip system with the electrical cables, which is beneficial for the miniaturization of the catheter.

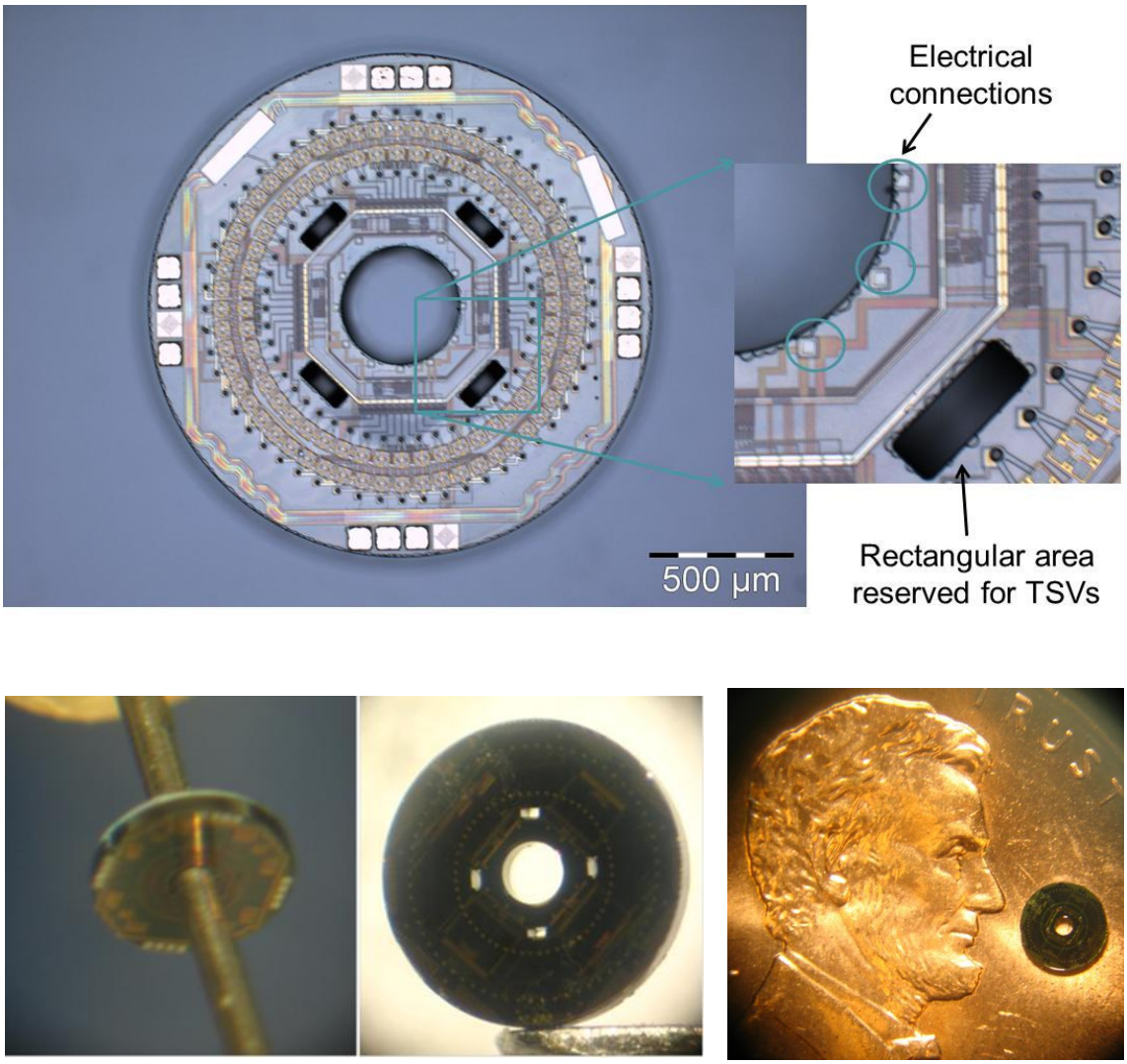


Figure 76. (Top) Picture of the IC after etching for the donut shape. (Bottom) Various pictures of the donut shaped ICs. On the right one, the IC is placed on a 1 cent coin.

4.4. Volumetric Imaging Results

For the imaging experiment, a target consisting of a 100-µm copper wire is placed 1.8 mm above the surface of the array (Figure 77-top). This target was placed into the water filled Petri dish. The Rx and Tx elements were biased at 80% of the collapse voltage. The width of the clk which is also used as the high-voltage pulse trigger is set as 30 ns. The low-voltage trigger pulse is amplified by the on-chip pulsers to generate a 25-

V pulse to the transmit elements. A 1.9x1.9x2.8 mm reconstructed volumetric image of the wire target is shown in Figure 77-bottom with a 25-dB dynamic range. Assuming a 20-µs pulse repetition rate for each A-scan, the data collection for the whole array (4096 A-scans through 4 parallel outputs) takes around 20 ms and therefore the image rate can be 50 frames per second. If a reduced set is used [156] the frame rate can be further increased.

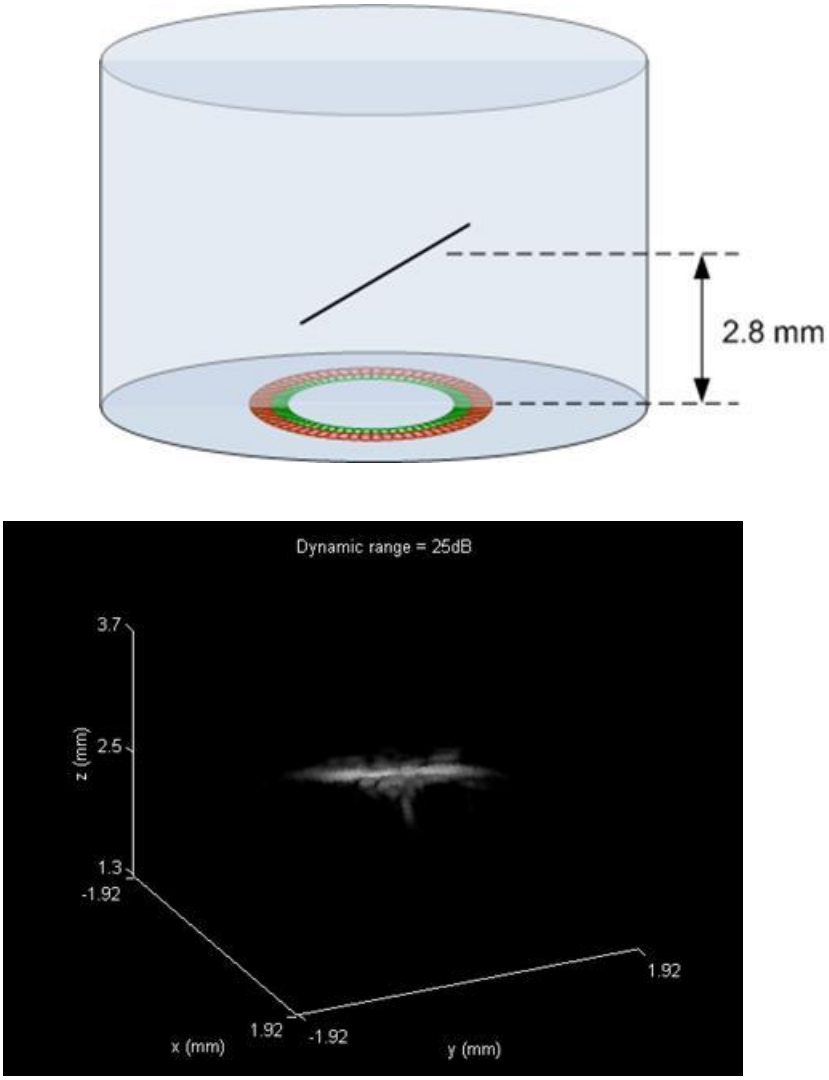


Figure 77. (Top) Schematic of the imaging setup consisting of a 100-µm wire target placed directly above the CMUT-on-CMOS dual-ring array. (Bottom) Volumetric display of the image of the wire target.

4.5. System-Level Comparisons with Previous Works That Closely Integrate CMUT Arrays with Electronics

Two example studies where front-end electronics are closely integrated with 2D piezoelectric arrays can be seen in [51, 157]. Similarly, a system that closely integrates custom transmitter and receiver electronics with a 2D CMUT array is demonstrated in [52]. However, this work is not targeted for IVUS or ICE imaging in particular. Therefore the size of the IC, which is not limited by the catheter size, is relatively large (10 mm x 6 mm). A forward-looking ICE imaging system based on a 1-D 24-element linear CMUT array (1.7 mm x 1.3 mm) integrated with an IC (2.1 mm x 2.1 mm) including both pulsers and receivers is shown in [113]. A similar IC (1.4 mm x 1.9 mm) designed for the same 1-D 24-element linear CMUT array only includes the receiver circuitry and provides ±50-V bipolar pulses externally from the imaging system [158]. A study for a 64-element CMUT ring array (2.5-mm outer and 1.6-mm inner diameter) implements an IC (1.0 mm x 1.2 mm) that also only includes receiver circuitry and excludes the pulsers [111, 158]. The IC used in these works is designed to interface with 8 transducer elements and therefore a total of 8 ICs are required for all of the 64 elements of the array.

Note that none of the above mentioned implementations are targeted for IVUS applications. The only commercially available IVUS system (side-looking) that integrates the ICs inside the catheter was discussed in section 1.4.3.2. This system uses amplifiers with an input-referred current-noise level around 1.3 pA/√Hz and on-chip transmitters provide 10-V pulses [44]. Compared to this commercial system, the 220-fA/√Hz input-referred current-noise level and the 25-V pulse system discussed in this chapter may

provide a 15x improvement in the system SNR. Also note that the system in [44] requires many connections between the array and the separate ICs, which make the catheter assembly very challenging.

The ring-array work in [111] that is targeted for a FL-ICE application is the closest one to the FL-IVUS application discussed in this chapter. Therefore, in this section this system is discussed in more detail. In [111] the integration with the CMUT array and the ICs requires through-wafer vias and depends on successful flip-chip bonding to a flexible PCB (flex-tape) through 244 solder interconnects. The bonding is done using 80-μm and 60-μm solder balls which consume considerable area. On the other hand, in our monolithic integration approach, the CMUT-IC connections are done through much smaller 25 μm x 25 μm metal areas. Also, as mentioned earlier, these CMUT-IC connections do not necessarily need to consume extra area because the connections can be done by only utilizing the topmost metal level which can be on top of the active CMOS circuitry. Considering that there is a need for 56Tx plus 48Rx connections, eliminating the area need for interconnects is very advantageous for this area limited application.

In [111], the system requires a total of 100 cables to provide all the electrical connections to the IC's partly because there is no multiplexing and all channels are carried out. On the other hand, the demonstrated single chip system in Figure 59 requires only 13 connections. In [111], since each transducer element is used for both transmit and receive, there is a need for a T/R switch for each transducer element. On the other hand, the dual-ring array shown in Figure 59 uses separate transducer rings for transmit and receive operations and therefore there is no need for a switch to isolate the transmitter-

receiver electronics. As mentioned earlier, eliminating the need for noisy protection switches helps on improving the noise. Also, eliminating the switches saves area in the layout as well, because otherwise the high-voltage protection circuitry could consume considerable area. For instance, in the work in [102], the protection circuitry consumes almost 1/3rd of the total 200 x 200 μm area for the pulser-receiver circuitry for a single transducer.

Finally, the area of a single IC in [111], which does not contain any pulser circuitry, is 1.0 mm x 1.2 mm and the system requires 8 of those ICs. Comparing that total area with the area of the 1.5-mm diameter IC in this work, which includes both pulser (for 56 elements) and receiver circuitry (for 48 elements), demonstrates the significant area improvement which is critical for the ultimate miniaturization of the system.

CHAPTER 5

NOISE BASED CHARACTERIZATION OF CMUTS USING LOW-NOISE RECEIVER ELECTRONICS

Although it contains valuable information about sensor and transducer systems, the thermal-mechanical (T-M) noise in ultrasonic and other mechanical transducers is mainly discussed in the context of lower limit for signal detection [159-162]. Ultrasonic transducer designs try to reduce T-M noise by minimizing losses in the system except for the unavoidable radiation losses. Electronics designs for imaging applications ultimately aim to detect signals down to T-M noise level but not much lower, because most of the cases they are limited by other design parameters such as power consumption and dynamic range. Consequently the information contained in the T-M noise spectrum of ultrasonic transducers is usually ignored.

However, when the transducer is modeled as an electrical network, the power spectral density of the current noise provides information about the admittance (impedance) of the transducer [163, 164]. This provides a passive means of characterizing transducers and transducer arrays especially when no electrical port is available for direct impedance measurement. Capacitive micromachined ultrasonic transducer (CMUT) arrays monolithically integrated with CMOS electronics is a very relevant example where the transducer outputs are directly connected to the inputs of the pre-amplifier electronics [164]. Therefore, observing the T-M noise at the output of the electronics can be very useful for testing CMUT array performance at a wafer level, before the array packaging is completed.

Furthermore, with low internal losses, the spectral properties of the real part of the electrical impedance of the CMUT would be dominated by its radiation characteristics. This in turn can be related to the models that simulate the full spectrum of waves generated by the transducer, including evanescent waves. Evanescent waves that are effective close to the surface of the transducer may not be identified in the radiation pattern measurements, but they significantly affect the acoustic cross talk in imaging arrays [165]. These wave modes have been utilized for sensing and actuation purposes and passive noise measurements can provide an alternative sensing technique for these applications [166, 167]. More recently there has been a renewed interest in using diffuse noise fields for passive imaging and sensing applications, especially for underwater acoustics and geophysical applications [168]. Since thermal-mechanical noise is an ideal diffuse noise source, it can be used for similar applications in the MHz range using suitable transducer arrays and electronics combinations [169, 170].

Motivated by this background, in this chapter we first relate the CMUT T-M noise to its electrical characteristics and determine the requirements on the electronics for T-M noise detection with high SNR. In previous chapters, it is shown that when CMUTs are monolithically integrated with custom-designed low-noise electronics, the output noise of the system can be dominated by the CMUT thermal-mechanical noise even for devices with low capacitance.

We use the T-M noise measured in air on CMUT arrays monolithically integrated with CMOS electronics to test functionality and uniformity of the intravascular imaging array elements. We demonstrate this method on the elements of an 800-μm diameter CMUT-on-CMOS array designed for intravascular imaging in the 10-20 MHz range.

Noise measurements in air show the expected resonance behavior and spring softening effects.

Noise measurements in immersion for the same array provide useful information on both the acoustic cross talk and radiation properties of the CMUT array elements. The measurement method can be exploited to implement CMUT based passive sensors to measure immersion medium properties, or other parameters affecting the electro-mechanics of the CMUT structure.

5.1. Thermal-Mechanical Noise of CMUT

A well-known mechanism for thermal-mechanical noise is the Brownian motion, which is the random vibration of microscopic particles caused by the collisions with the atoms and molecules in the surrounding material. Because of the energy dissipating mechanism in the system, there has to be a fluctuation force associated with the damping term to sustain these thermal vibrations. The spectral density of that force associated with the damper in the system (i.e. mechanical resistance) is given by [159]

$$\overline{F_{T-M\ NOISE}}^2 = 4kTR \tag{51}$$

where k is Boltzmann's constant (1.38 x 10^{-23} J/K), T is the temperature of the environment in Kelvin and R is the mechanical resistance. Note that, this expression is a direct physical analog to the Johnson-Nyquist noise in the electrical systems [171], which states that the spectrum density of the thermal voltage noise of any network is proportional to the real part of the impedance of the network. Similarly, the Norton-equivalent current noise is proportional to the real part of the admittance of the network.

The simple equivalent circuit for a CMUT element, along with the equivalent noise force (F_{NOISE}) associated with the real part of the total complex mechanical impedance is shown in Figure 78. As discussed in section 1.3.2, the terms on the mechanical side can be transferred to the electrical domain using the transformer ratio (Figure 79). In Figure 79 the noise term is represented with a Norton-equivalent current source. The equivalent CMUT electrical impedance is represented as $Z_{CMUT,MEC}/n^2$ where $Z_{CMUT,MEC}$ is the total impedance on the mechanical side that includes the radiation impedance ($Z_{RAD}S$), the membrane impedance ($Z_{MEM}S$) and any other mechanical losses. The spectral density of the thermal-mechanical current noise of CMUT can be given as

$$\overline{\iota_{CMUT}{}^2} = n^2 \frac{\overline{F_{NOISE}{}^2}}{\mathrm{Mag}\left(Z_{CMUT,MEC}\right)^2} = n^2 4kT \frac{\mathrm{Re}\left(Z_{CMUT,MEC}\right)}{\mathrm{Re}\left(Z_{CMUT,MEC}\right)^2 + \mathrm{Im}\left(Z_{CMUT,MEC}\right)^2} \tag{52}$$

where Mag, Re and Im denote the magnitude, real and imaginary parts of the complex impedance. The electromechanical transformer ratio (n) of the transducer is equivalent to $V_{DC}C_0/g$ where V_{DC} is the applied DC bias voltage, C_0 is the capacitance of the CMUT and g is the gap between plates.

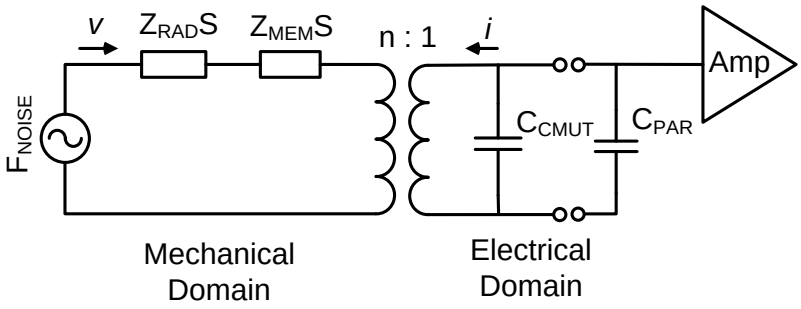


Figure 78. Equivalent circuit model for the CMUT element in receive mode. The thermal-mechanical noise is represented with a force term on the mechanical side. Units of Z_{RAD} and Z_{MEM} is in rayls and S is the area of the transducer. On the electrical side spring softening capacitance is omitted.

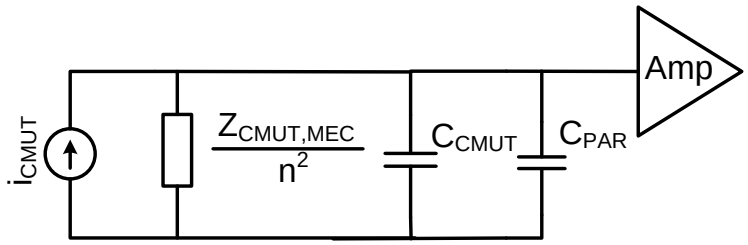


Figure 79. Simplified Norton equivalent circuit of CMUT where all the elements on the mechanical side are referred to the electrical domain.

Noticing that the current noise expression in (52) includes the admittance ($Y_{CMUT,MEC}$) term, the CMUT noise can simply be written as

$$\overline{\iota_{CMUT}{}^2} = n^2 4kT\mathrm{Re}\left(Y_{CMUT,MEC}\right) \tag{53}$$

To simplify the expression one step further, the equivalent impedance of the CMUT on the electrical side $\left(Z_{CMUT,MEC}/n^2\right)$ can be referred as $Z_{CMUT,ELEC}$. In that case the CMUT current noise in (53) can be rewritten as

$$\overline{\iota_{CMUT}{}^2} = 4kT\mathrm{Re}\left(Y_{CMUT,ELEC}\right) \tag{54}$$

It is evident that the noise expression simply gets the form of the Johnson-current noise associated with the real part of the admittance of the CMUT equivalent circuit.

To a first order, $Z_{CMUT,ELEC}$ can be assumed to be equivalent to a series RLC circuit. In that case, at the respective resonance frequency of the medium, the CMUT equivalent impedance can be assumed to be purely resistive ($R_{CMUT,ELEC}$). It follows that at resonance frequency, $Y_{CMUT,ELEC}$ in (54) becomes $1/R_{CMUT,ELEC}$ and hence CMUT current noise can be expressed as

$$\overline{\iota_{CMUT}{}^2}_{(\omega=\omega_0)} = \frac{4kT}{R_{CMUT,ELEC}} \tag{55}$$

Note that, the single RLC equivalent circuit assumes a single Q device and does not take the crosstalk effects into account. A more accurate estimation of the actual CMUT noise can be obtained by using a CMUT finite-element model and the general noise expression given in (52). However, the expression in (55) is suitable for a back of the envelope calculation to get a rough expected number for the CMUT noise to be used as a design consideration for the receiver amplifier design. For instance, $R_{CMUT,ELEC}$ value in immersion was calculated to be around 1 MΩ for the particular FL-IVUS array elements that are used in the noise dominated system discussed in Chapter III. Based on (55) this value entails an expected CMUT T-M noise current of 125 fA/√Hz.

5.2. Noise Measurements with CMUT Array

To accurately measure the CMUT noise level, the preamplifiers should be custom designed with a current noise low enough not to dominate the transducer noise.

5.2.1. Noise Measurements with CMUT Array Wirebonded to Low-Noise Electronics

We initially designed a resistive-feedback transimpedance amplifier with 20-kΩ gain in 0.5-μm CMOS and integrated that with a forward-looking CMUT array element using wirebonding (Figure 80). CMUT element is 70 μm x 70 μm consisting two membranes of the same size. The noise of the system in air is measured at different CMUT bias voltages using a spectrum analyzer (Figure 81). Input current noise is obtained by dividing the measured TIA output noise by the TIA gain. It can be seen that for zero bias voltage, system only demonstrates noise due to electronics. As the CMUT is biased closer to collapse the coupling coefficient increases and the amount of output noise associated with CMUT increases. It can also be seen that as the DC bias increases the noise peaking frequency decreases due to a well-known spring softening mechanism that shifts the resonance frequency.

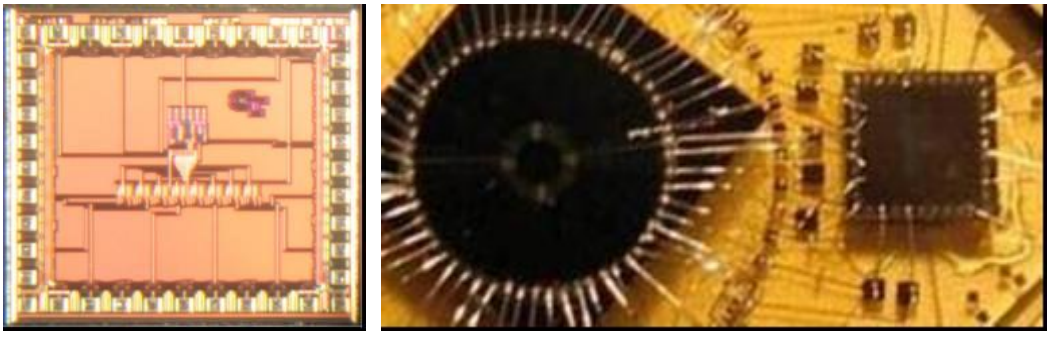


Figure 80. (Left) Picture of the IC in 0.5-μm CMOS; (right) receive amplifier is wirebonded to the forward looking array CMUT element.

The real part of the electrical impedance of the same CMUT element used in the noise measurements are measured with a network analyzer at different bias voltages (Figure 82). The real part of the CMUT impedance peaks at the resonance frequency of

the transducer which is also the same frequency where the noise measurement peaks. This clearly demonstrates that noise measurements in air provide direct information of the impedance and resonance frequency of the CMUT.

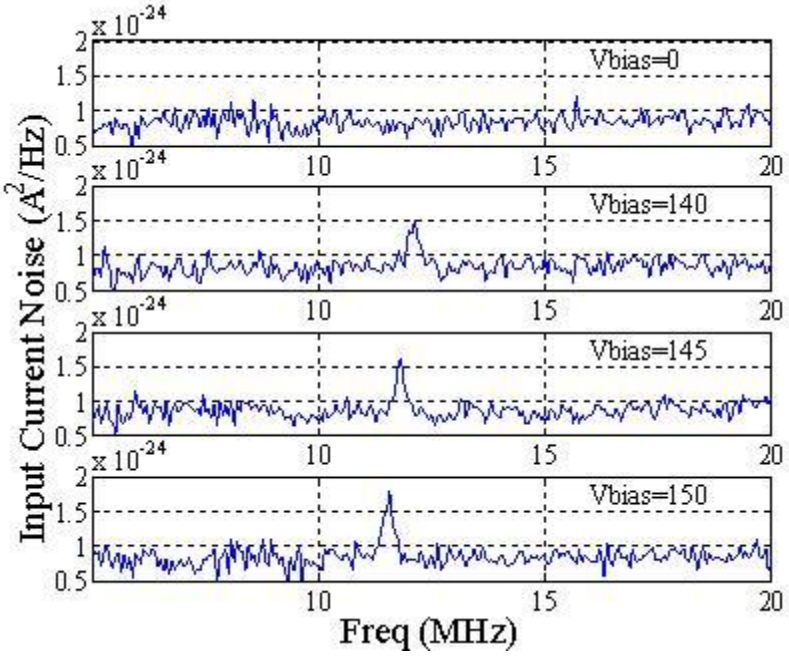


Figure 81. Noise of the CMUT and wirebonded TIA system with different CMUT biases

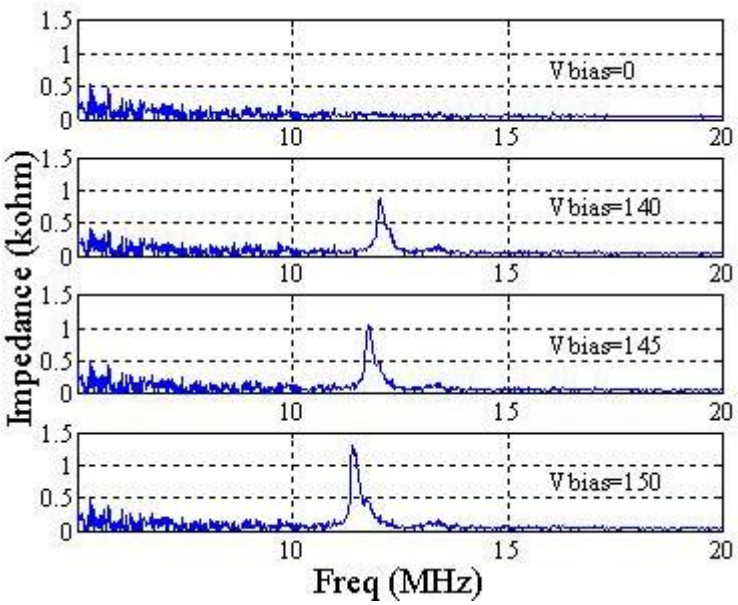


Figure 82. Real part of the CMUT impedance with increasing bias voltages.

The integrated array is also placed in water for noise measurements in immersion however; the noise spectrum didn't show any significant change for increasing CMUT bias voltages indicating that wirebonded TIA noise is not low enough to measure CMUT noise in immersion. The TIA design optimized for monolithic integration, which is used for the measurements presented in the following section and section 3.6.4 has around 20 dB better noise performance compared to the 20-kΩ feedback design used in the wirebonding case discussed here.

5.2.2. Noise Measurements with CMUT Array Monolithically Integrated with Low-Noise Electronics

In section 3.6.4, a CMUT noise dominated system is demonstrated through output noise measurements of the system performed with CMUT elements in immersion (Figure 51). One critical observation in Figure 51 is that the source of the additional features in

the noise spectrum between 5 MHz and 10 MHz is the evanescent waves trapped over the array. This suggests that the T-M noise provides useful information on both the acoustic cross talk and radiation properties of the CMUT array elements. This can be used to measure properties of the immersion medium that changes that cross-coupling behavior, or other chemical or physical inputs affecting the electromechanical properties of the CMUT membrane.

The same monolithically integrated transimpedance amplifier design is also used for noise testing of CMUTs in air. As mentioned earlier for air coupled applications, bandwidth is not a concern. Therefore, for noise testing in air, a charge [125] or an open-loop voltage amplifier can be more advantageous in terms of noise performance compared to the transimpedance amplifier since these amplifier topologies do not incorporate any feedback network noise.

For airborne applications the equivalent resistance at resonance frequency is roughly equal to the mechanical membrane losses which is much smaller compared to the real part of the radiation impedance. Considering (55), the smaller resistance in air applications implies that, at the corresponding resonance frequency, the noise level of the CMUT in air is higher than the noise of the CMUT in immersion. Therefore although it is not specifically designed for air application, this particular TIA front-end is also low-noise enough for CMUT noise measurements in air.

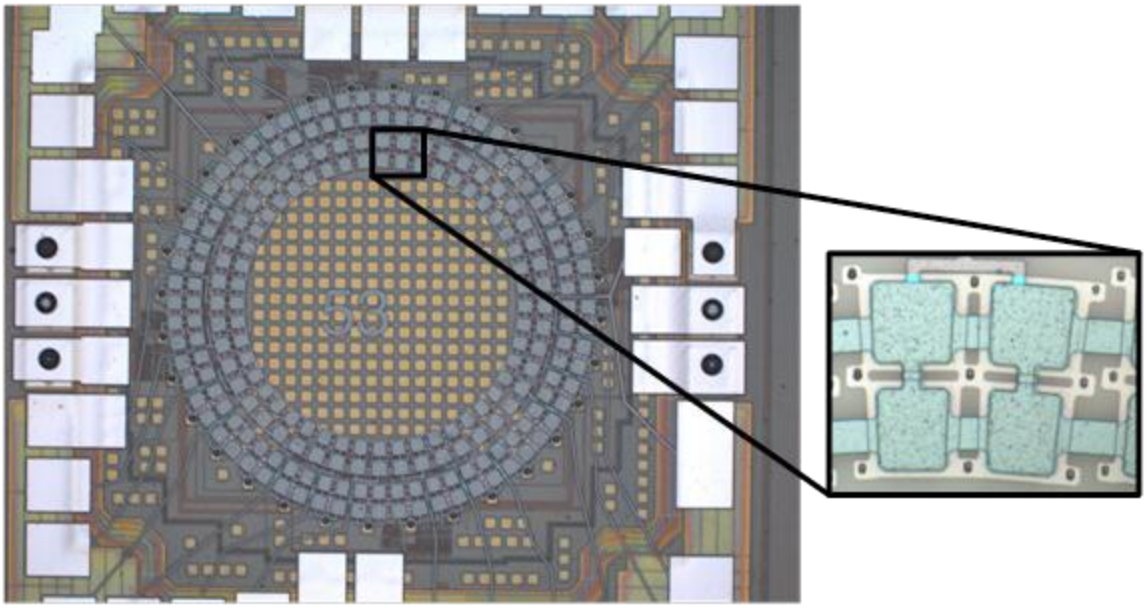


Figure 83. Micrograph of the dual-ring CMUT-on-CMOS array used for noise measurements, demonstrating the presence of two slightly different sized membranes in each element

Figure 84 shows the setup that is used to measure the noise output of the CMUTs. There are additional voltages (i.e. vdd, gnd and some control lines) applied to the CMOS circuitry, which are not explicitly shown in the figure. It is important to note that no external high-voltage pulse is applied to the CMUT element. The noise measurement method only applies a static DC bias to the CMUT element and the noise spectrum is measured at the output of the receive electronics.

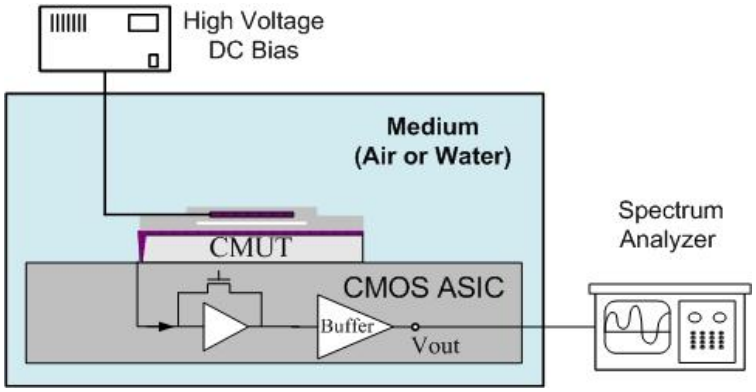


Figure 84. Illustration of experimental noise testing setup used to measure input current noise of a CMUT receiver element

The noise spectrum of the system in air is measured at the output of the receive amplifier using an Agilent 4395A Spectrum Analyzer. CMUT element is biased at various increasing voltages (Figure 85). The measured noise at 0 V is due to the noise of the receiver electronics. As the CMUT bias voltage is increased the CMUT noise emerges. As shown in Figure 83, each CMUT element contains two pairs of trapezoidal membranes with slightly different sizes, which results in the two main resonance peaks in the noise measurements in air.

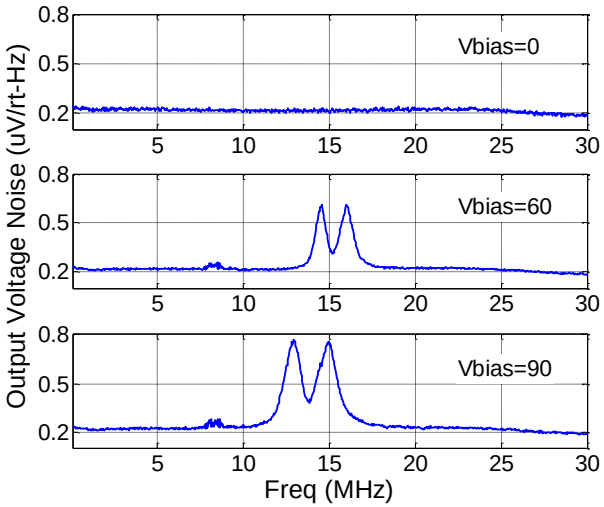


Figure 85. Measured noise of the monolithically integrated system in air with CMUT biased at 0V, 60V and 90V. As CMUT bias is increased the resonance peak shifts to lower frequencies due to spring softening effect.

Figure 86 plots the noise measurements of 4 different CMUT elements on the array in Figure 83 connected to 4 dedicated TIAs. The CMUT-TIA pairs are scanned using the multiplexer on the chip to investigate array functionality and uniformity in air. For this measurement CMUT elements are biased at 60 V. It can be seen that the resonance peak frequencies are uniform among the array elements.

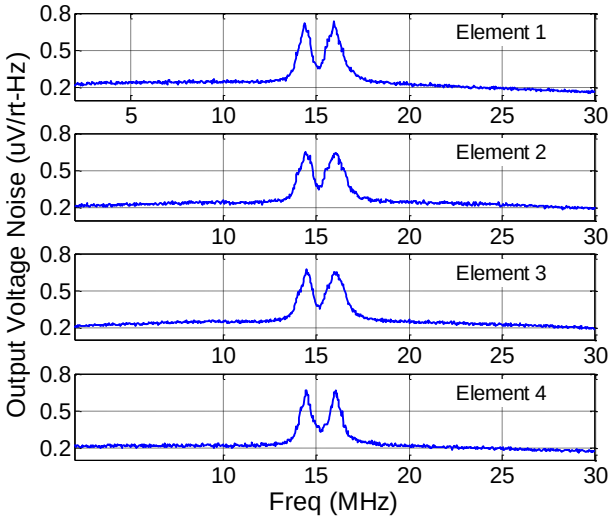


Figure 86. Measured input current noise from 4 monolithically integrated CMUT elements and TIAs.

These results demonstrate that noise measurements in air can be used to easily characterize the functionality of the receive circuitry and the CMUT array; the uniformity around the CMUT array elements and to verify the proper interconnection between the array and receiver electronics. This is important because this noise-based method can be used for wafer level testing of the devices after the monolithic integration is complete and before any packaging or immersion effort. Without such a method it would be very challenging to test the integrated device. Once one of the CMUT electrodes is directly connected to the receive amplifier, measuring the impedance of the CMUT elements using a network analyzer for characterization is not an option because that type of measurement would require access to both of the electrodes. One should note that the noise-based characterization method uses receive amplifiers already existing in the catheter for the imaging application; therefore it doesn't require any additional power consumption or chip area.

When the CMUT current is sensed with an amplifier with finite input impedance, the amplifier input impedance forms a current divider network with the CMUT impedance and the impedance of the total capacitances at the input. This slightly reduces the measured peak noise magnitude in air however it does not change the measured peak frequency. On the other hand, for operation in immersion, the equivalent CMUT impedance is typically much higher compared to the amplifier input impedance. Therefore it can be claimed that in immersion almost all of the current generated by the CMUT flows through the amplifier and is sensed.

5.3. Possible Methods for Readout of the Noise

Noise measurements are traditionally done with a spectrum analyzer. However, spectrum analyzer is a bulky and expensive instrument. Alternatively, output of the integrated system can be connected as an input to a tunable band pass filter. The pass band of the filter can be electronically swept to determine at which frequency the noise peaking occurs.

Another method can use a band pass filter with well-defined cut-off frequencies and utilize the spring softening effect of the CMUT. It can be seen from Figure 81 that as the dc bias increases the resonant frequency shifts to lower frequencies. Therefore the noise peaking frequency can be shifted using CMUT bias voltage and output noise can be readout with the band pass filter with constant cut-off frequencies.

5.4. Conclusions

The T-M noise of the CMUTs, even small elements with capacitances in the sub-pF level, can be measured using low noise CMOS integrated electronics. This noise spectrum can be directly related to the real part of the admittance of the CMUT using well known theorems. When performed in air, T-M noise measurements provide a novel way for testing functionality of CMUT array elements as well as the monolithically integrated electronics. As CMUTs behave as lightly damped resonators in air, distinct resonance peaks in the T-M noise spectrum and their frequency shift with DC bias provide accurate information on the CMUT characteristics. In immersion, the T-M noise spectrum contains information that is not readily available in a typical pulse-echo response. This is because the T-M noise spectrum reveals the effect of both evanescent waves trapped over the array and acoustics waves radiated away from the array on the admittance of the CMUT elements. Consequently, once the CMUT is well characterized, the T-M noise spectrum can be used to measure certain characteristics of the immersion fluid, providing an alternative to impedance based active CMUT fluid sensors.

CHAPTER 6

BEAMFORMING FOR HIGH-FREQUENCY IVUS

Beamforming is a term that is related to phased-array systems and it refers to the operation of generating appropriate delays to steer and focus the received and transmitted signals to increase the image quality. To synthesize new focus points, the applied delays are changed accordingly. The need to generate delays dedicated to each receive and transmit channel increases the complexity and makes it a big challenge to meet the size and power consumption requirements of the front-end system for a catheter-based application. Delay implementation is especially challenging at high frequencies because it is difficult to modify the beamforming methods that are used at lower frequencies for higher frequency operation. This complexity of implementing high-speed delay circuitry has been one of the major limitations in development of catheter-based dynamically-focused high-frequency ultrasound array systems.

A catheter-based application can only tolerate a limited number of cable connections and this introduces an additional constraint on the beamforming implementation. Having the beamforming circuitry external to the body is impractical because that requires several (as many as the number of transducer elements) cable connections between the array and the external beamformer. Therefore, implementing beamforming delays on an integrated circuit adjacent to the transducer array inside the catheter probe is critical mainly because it reduces the required number of cables. This also eliminates the need for many high-speed output drivers and simplifies the packaging requirements. Note that the need for having the beamforming circuitry inside the catheter

places a strict power budget limitation to the front-end system because as discussed earlier, the feasible power dissipation in the catheter is limited to a few hundred miliwatts. In the below discussions and comparisons of various beamforming approaches, this requirement of having the beamforming circuitry inside the catheter while complying with the power dissipation limit is considered as an important criteria in the final choice of the beamforming implementation.

6.1. Beamforming Approaches for High-Frequency Arrays

On the receive side, the required beamforming delays can either be implemented in the digital domain after sampling the signal or by analog methods. The very first beamformers in medical ultrasound were based on analog methods however with the significant advances in digital CMOS technology, the beamforming started to shift to digital methods, which provide a greater flexibility and accuracy in the delay implementation. Currently majority of the ultrasound beamformers are implemented in digital domain [172]. On the other hand, after the discussion in this section it will be concluded that for this particular catheter-based high-frequency side-looking IVUS application, analog beamforming is a better suited approach. In the following sub-sections, various methods and trade-offs for delay implementation for receive beamforming in high-frequency catheter arrays are discussed in detail.

6.1.1. Beamforming Using Conventional Multi-Bit ADCs

In digital beamforming, echo signals from each channel of the sensor array are sampled using a dedicated A/D converter (ADC). After the incoming signals are digitized

typically they are written into first-in, first-out (FIFO) registers and are then read out with different starting times to accomplish the time delays. Evidently, in digital beamforming, many high speed, high resolution ADCs are needed, which significantly increases the power consumption of the system. In comparison, in analog beamforming the signals are beamformed first and a single ADC is required to digitize the beamformed signal.

In beamforming approaches that utilize sampling (either analog or digital), the sampling rate determines the minimum delay increment because signals can be delayed with time increments equal to the sampling period. The discrete-time-increment delay results in delay-quantization error and causes grating lobes in the image. To maintain acceptable levels of grating lobes and adequate delay accuracy, the delay resolution must be at least on the order of 1/20th of the wavelength of the main signal [173, 174]. Implementing sampling rates at 20 to 30 times the ultrasound signal frequency demands excessively high sampling speeds from multi-bit ADCs, which would require unacceptably high power consumption to obtain enough resolution at those high speeds [175]. For instance, for a 50-MHz application, to achieve the required finely delayed samples, the sampling frequency should be at least at 1-GHz rate. Therefore, to relax the high sampling rate requirement of the multi-bit ADCs while achieving the required delay accuracy, the required delays are typically separated into coarse and fine delay components. Relatively lower speed ADC's with sampling rates of four to eight times the ultrasound carrier frequency are used to generate coarse delays. Fine delays are typically generated using digital interpolation to up-sample the digitized samples to obtain new samples at the appropriate fine delay points. In an alternative fine delay generation method, the RF signal is mixed to a complex baseband signal and fine dynamic delays are

implemented using adjustable phase rotation [173]. The downside of both of these fine delay implementation methods is that they both use noisy and complicated processing steps to synthesize accurate delays. As the channel counts increase the hardware complexity and the required digital processing to implement the beamforming becomes substantial and increases the cost.

Conventional multi-bit ADC-based digital beamformers are demonstrated for high frequency linear [176-178] and annular ultrasound arrays [179-181]. However, these beamformers are based on big PCB boards including many ADCs that are packaged separately in multichip modules. In addition, FPGAs are used for further digital delay processing. Because of the sheer size of these systems, they are not suitable for integration inside a catheter. Furthermore, conventional multi-bit ADCs are power hungry. Even if the packaging and interconnect problems are resolved, due to the very strict power budget limitations of the catheter application, including a power hungry ADC for each element inside the catheter is not feasible. In [182, 183] to reduce the power consumption, a single 250-MHz sampling-frequency ADC with a power consumption of 270 mW is shared among many receive channels however it should be noted that this approach increases the data acquisition time and reduces the frame rate.

6.1.2. Beamforming Using Delta-Sigma Oversampling ADCs

Challenges with conventional multi-bit ADCs can be overcome and the front-end can be simplified by using a Delta-Sigma (ΔΣ) ADC. In ΔΣ beamforming, incoming signals are digitized by using single-bit ΔΣ oversampling modulators. Oversampling at high frequencies removes the necessity for complicated fine delay generation methods. In

addition, ΔΣ modulators consume significantly less power compared to Nyquist-rate ADCs, because they generate only a single bit of resolution. Because of these advantages, low-power single-bit oversampling ΔΣ ADCs have been found attractive to implement low-cost beamforming systems for narrowband ultrasound applications [184-192]. Note that, the referenced studies that discuss IC implementations for the ΔΣ beamforming approach for ultrasound applications are limited to low frequencies (~5 MHz) [189]. This is because use of ΔΣ beamforming is unfeasible for high frequency (~50 MHz) ultrasound applications due to the need for extremely high over-sampling rates. Even state of the art ΔΣ ADCs don't meet the sampling speed requirements for a 50-MHz application while maintaining acceptable power consumption.

The above discussions for multi-bit and ΔΣ ADCs indicate that both in terms of power and delay accuracy requirements, beamforming approaches using signal sampling such as digital beamforming are not practical for high-frequency delay generation inside the catheter. This clearly motivates the use of analog methods, which are discussed in the next section.

6.1.3. Analog Beamforming

Analog beamforming is typically done by separately implementing coarse and fine delays [193, 194]. There are two conventional methods for fine delay generation. The first method is using a tapped delay line where delays are selected with complex switching circuitry to select the appropriate tap for a particular channel. A major drawback of this approach is that the numerous cross-point switch matrices and the excessive number of taps make this approach bulky. In addition, the switching transients

that occur during the change between different taps make the approach noisy. In the second method of implementing fine delays, the delay is approximated by a constant phase shift. In this method the received signal from each channel is modulated to baseband or to an intermediate frequency by multiplying with a mixing signal and adjustable phase rotation is applied [195]. This method eliminates the need for multiple tap delay lines and cross-point switches. On the other hand, this phase shift method is not suited for wideband delay generation because the phase shift approximates the true delay accurately only within a limited bandwidth [51].

The coarse component of the delay is typically generated using a tapped delay line preceded by a switch circuit. Alternatively, coarse delays can be implemented using the sampling period of an ADC [51]. This method is referred as hybrid beamforming since it uses both analog (for fine delay) and digital (for coarse delay) techniques.

The delays in an analog beamformer can be implemented using any discrete or continuous-time analog methods which are discussed in further detail below.

6.1.3.1. Discrete-Time Analog Delay Generation

The sampled-charge circuits such as bucket-brigade device (BBD) [196] and charge-coupled device [197] are proposed in literature. BBD devices are CMOS compatible but they suffer from poor charge-transfer efficiency. CCDs have better performance compared to BBDs but require special process steps and therefore are not compatible with standard CMOS processes. In addition, power dissipation is a significant issue for CCDs switching at high rates [51].

Another discrete-time analog beamformer approach is using serial analog memories that are proposed in [198-200]. This method is also a discrete time solution and

may be difficult to implement at high frequencies because of the aforementioned need for very high sampling rates. Switching noise become more significant as the clock frequency is increased. In addition, the switch control signals have the potential of producing spectral components in the signal bandwidth creating a pattern noise in the final image [51].

Another common way of delay implementation is using a sample and hold chain, where delaying is achieved by passing the signal through a chain of samplers. Because of the numerous unity gain buffers, this method draws considerable power and consumes significant real estate [51]. In addition, the noise, harmonic distortion and dc offset introduced by each stage gets accumulated as the signal passes through the chain [201].

6.1.3.2. Continuous-Time Analog Delay Generation

Continuous-time analog methods are advantageous compared to time-discretized solutions because there is no sampling or quantization of the waveform. There are various means of continuous-time analog delay generation. A conventional method is to use a lumped LC delay line architecture [202] however this method is not feasible due to the poor quality factor (Q) of inductors in standard integrated circuit processes. Alternatively, a continuous-time analog delay can be implemented using low-pass or all-pass filters. In the next chapter, there is a section that discusses the advantages and limitations of various low-pass and all-pass filter delay approaches in detail and therefore that discussion is not repeated here.

6.2. Unit-Delay-Based Dynamic Receive Beamforming Architecture for Annular Arrays

Figure 87 illustrates the beamforming scheme focusing on the main axis of the annular array. Notice that in annular arrays steering is not implemented and focusing is done only on the main axis. Also, note that the center element should be delayed the most since the returning echoes arrive at the center element the earliest.

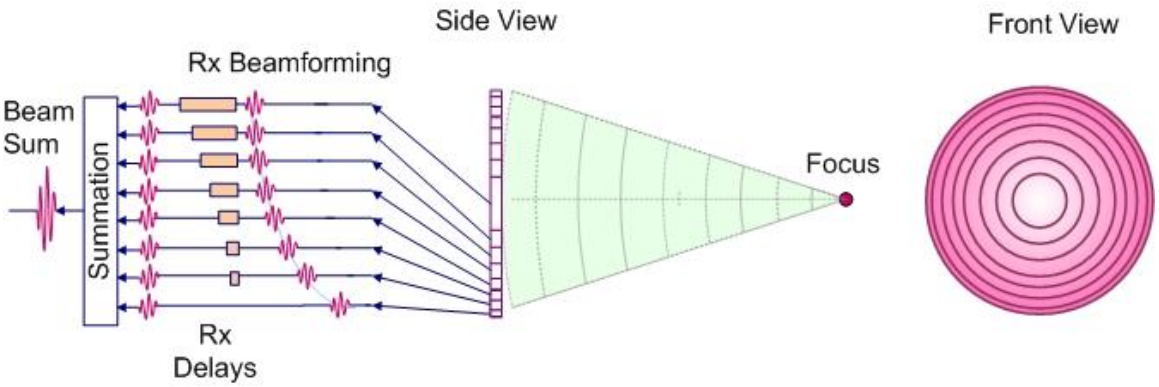


Figure 87. Receive beamforming for annular array. For receive beamforming received signals are delayed so that signals arriving from the desired focus point adds coherently in time.

Annular arrays are usually designed with equal-area transducers to maximize the axial pressure [55]. In an equal-area annular array, the relative delays between the adjacent channels can be approximated to be equal to a constant delay. In other words, such an annular array performs non-uniform spatial sampling of circular wavefront received on the planar surface of array in such a way that the detected sampled wavefront becomes linear across the array elements.

A clever beamforming strategy specifically developed in [124, 203] for equal-area annular arrays employs this fact to implement a focusing architecture using a collection

of identical analog delay stages that are simultaneously adjusted to accomplish dynamic focusing on the axial line.

Assume the case for an N element equal-area annular array focusing to f (Figure 88).

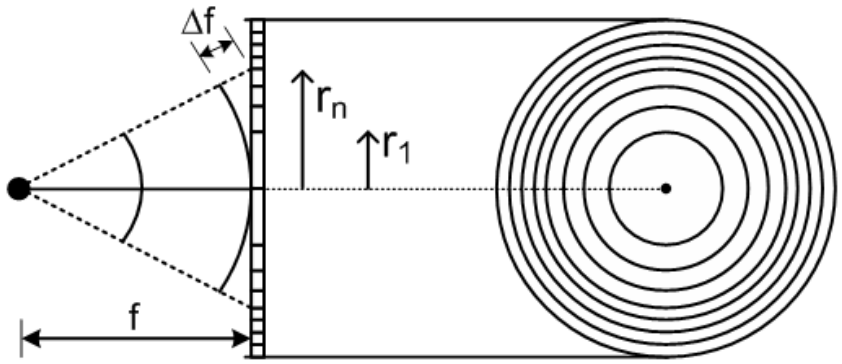


Figure 88. An equal-area annular array focusing to a distance f. The path delay between elements is denoted as Δf (adapted from [203])

$$\Delta f = \sqrt{r_n^{\,2} + f^{\,2}} - f \tag{56}$$

$$\frac{\Delta f}{f} = \sqrt{\frac{r_n^{\,2}}{f^{\,2}} + 1} - 1 \tag{57}$$

Assuming $r_n^{\,2} << f^2$,

$$\Delta f = \frac{r_n^{\,2}}{2f} \tag{58}$$

In this case, the necessary delays to focus the array at a distance of f lead to the relation

$$\tau_n = \frac{r_n^{\,2}}{2fc} = \frac{nr_1^{\,2}}{2fc} = n\tau_u \ \ (\tau_u = \frac{r_1^{\,2}}{2fc} \, is\, unit\, delay)\ , \tag{59}$$

where r_1 is the radius of the central element, r_n is the radius of the nth element, c is the speed of sound and n is the array element number [203]. Here the unit delay element, τ_u, is independent of the channel number. In Figure 89, the unit-delay based beamforming approach is illustrated for a representative 3-element annular array. It can be seen that the focal distance can be displaced along the image axis dynamically by tuning the unit delay (τ_u) value. The figure illustrates that the focal point gets closer to the array when the unit delay is increased from τ_1 to τ_2.

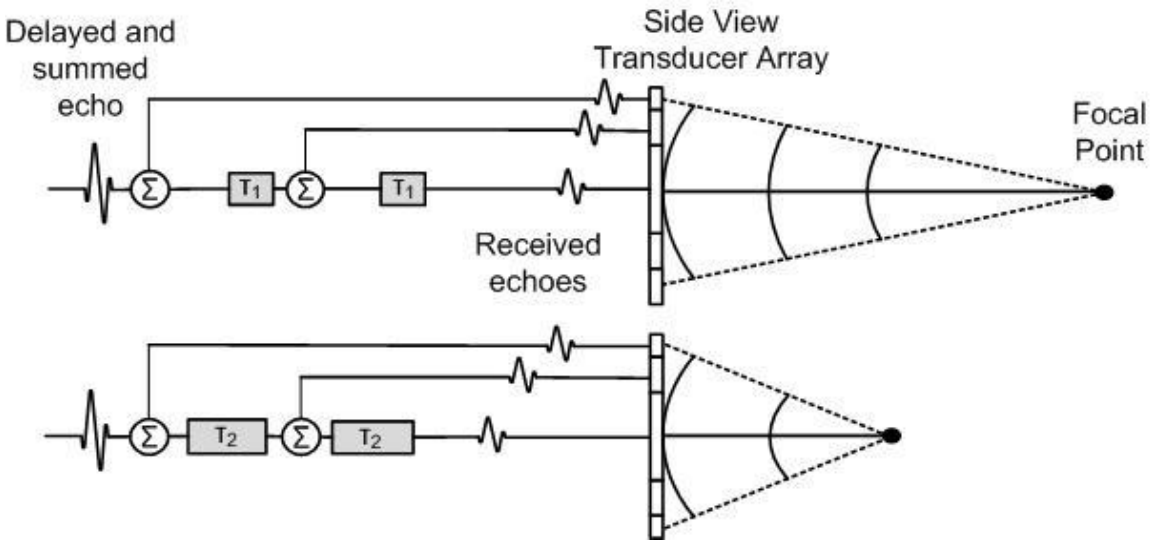


Figure 89. Unit-delay based dynamic receive beamforming scheme for a representative 3-element annular array. A unit delay that can implement variable delays is controlled to change the focal point. In this figure, two different focal points corresponding to two different unit delay values are depicted.

The figure shows the architecture for 3 elements but it is clear that an 8-element annular array would require 7 delay stages. It can be seen that this unit-delay-based beamforming scheme is very compact. In addition, since the delays of the unit-delay stage is variable, there is no need for switching of the delay taps (which is the case for a tapped delay line) to modify the focal point. Furthermore, in this application there is no

need for separating the delays to coarse and fine delay components because the required delay range is not very high, i.e. the required maximum delay is around 2.5 times the minimum required delay.

The accuracy of the assumption of $r_n^2 << f^2$, which leads to (58), drops for focusing distances that are close to the array aperture. This results in an error between the exact (ideal) delays and the truncated delays that are approximated by (59). To test the effects of quantized delays on the image quality, simulated beam patterns using both exact and quantized delays are produced. The simulated two-way (pulse-echo) lateral beam patterns at f#2 are shown in Figure 90. Here the exact and the truncated delays for f#2 (see Table 9) are employed. The exact delays in Table 9 are calculated considering the center of mass of the elements (in an 8-element 800-μm diameter annular array) as element center. In the simulations a 20-MHz Gaussian pulse with 60% FBW is used. Figure 90 shows that the main lobes of the beams produced with exact and quantized delay patterns are nearly identical, while the quantized delays, as expected, result in raised near side lobe level (at -45 dB). Since the side lobe level with truncated delays is still below -40 dB, the discussed beamforming architecture should be acceptable for IVUS applications.

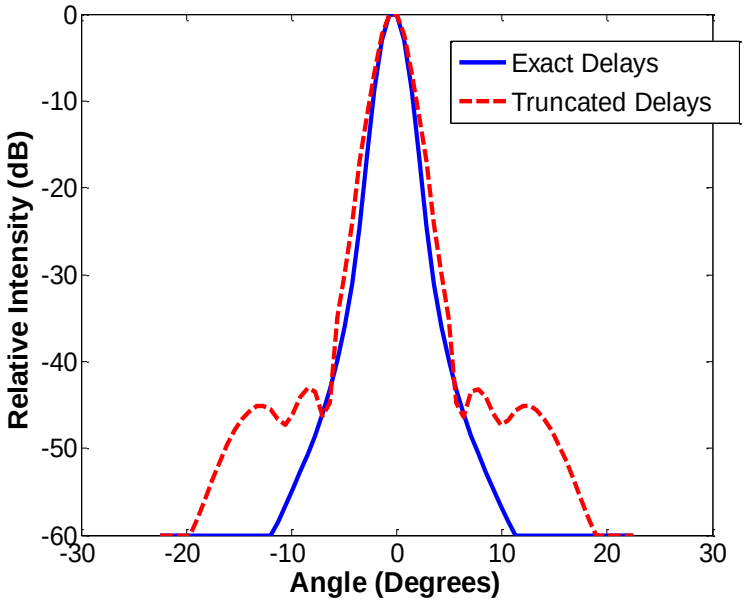


Figure 90. Point spread functions (PSFs) with exact delays and truncated delays. The side-lobe level stays less than 40 dB for truncated delays which is acceptable for IVUS imaging.

Table 9. Truncated unit-delay values to focus @ f # 2

Element Number	Exact Delays (ns)	Truncated Delays (ns)
8 (outermost)	0	4.2 x 0 = 0.0
7	4.47	4.2 x 1 = 4.2
6	8.59	4.2 x 2 = 8.4
5	12.36	4.2 x 3 = 12.6
4	16.22	4.2 x 4 = 16.8
3	20.62	4.2 x 5 = 21.0
2	24.43	4.2 x 6 = 25.2
1 (centermost)	28.58	4.2 x 7 = 29.4

Figure 91 plots the required unit-delay values to dynamically sweep the focal range of an 8 equal-area element 800-μm diameter array from f#1.7 to f#4.1 based on the approximation in (59). As the time increases the required delay values are reduced to move the focal point away from the array in accordance with the location of the wavefront. The figure indicates that to sweep between the specified focal ranges the delay values should be decreased from 5 ns to 2 ns within approximately 2.8 μs (1.7 μs to 4.5 μs).

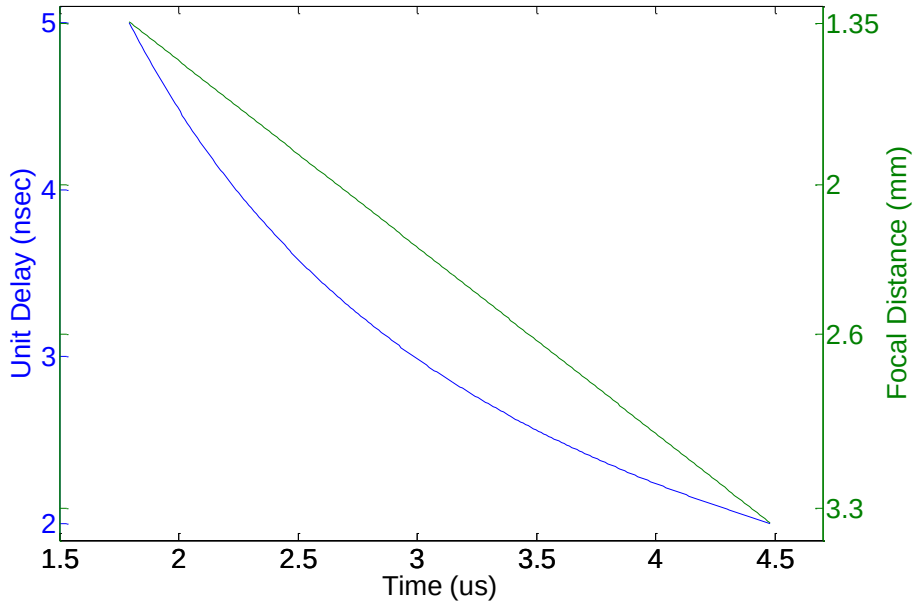


Figure 91. Required unit-delay values to dynamically sweep the focal range of an 8-element 800-μm diameter array from 1.35 mm to 3.3 mm based on the approximation in (59). To sweep between those focal ranges the delay values should be decreased from 5 ns to 2 ns within approximately 2.8 μs (1.7 μs to 4.5 μs). The focal distances of 1.35 mm and 3.3 mm corresponds to f#1.7 and f#4.1 respectively.

Focusing to axial ranges very close to the array is not practical because the echoes coming from any target that is very close to the array are not detectable by the array because of the transducer ring-down effects. Similarly, focusing in the far-field of the

array does not considerably improve the image quality either. As a numerical example, the far field for an 800-µm diameter array starts around 4 mm. The range of the focal sweep depends on the range of the delays that the delay cell can generate and typically a focal range slightly larger than an octave should be enough to cover the useful dynamic focusing range.

Among the various delay approaches discussed in section 6.1.3, a continuous-time all-pass filter is chosen as a viable delay method for the implementation of the discussed unit-delay cell required for the beamforming architecture. The realization of the delay cell with a current-mode circuitry is discussed in detail in the next chapter. It should be mentioned that achieving uniform linear delay with respect to frequency is a challenge using continuous-time analog delay filters and this prevents implementation of long delays using analog filters. For instance, as will be discussed in the next chapter, the upper delay limit of a first-order all-pass filter for 50 MHz frequency is 2.5 ns. Therefore, if the required unit stage delay of this application was around tens of ns, then the total noise and power of the delay line based on an analog filter approach could be a significant concern. In that case, despite its above-mentioned drawbacks, a discrete-time analog solution such as the one discussed in [200] could be a more feasible approach. However, as shown in Figure 91, in this side-looking high-frequency IVUS application, the maximum required unit-delay of the beamforming architecture is around 5 ns, which makes the use of an analog-filter-based approach feasible.

CHAPTER 7

ANALOG BEAMFORMER INTEGRATED CIRCUITS FOR HIGH-FREQUENCY IVUS

High frequency operation is desired to obtain better resolution and thereby to improve the image quality. However, as discussed earlier, there are two main challenges in implementing high-frequency array systems. The first one is the limitations of the current piezoelectric transducer technology in realizing finely-spaced elements required for high-frequency systems. As suggested in section 1.4.5, this barrier can be overcome using CMUT technology. An equally important impediment of the development of high-frequency catheter-array systems is the difficulties in the implementation of high-frequency beamforming in a power and area efficient manner within the catheter.

For the side-looking IVUS application based on annular arrays, minimizing the number of cables is essential because that is a rotating system and having many cables challenges the overall manufacturing of the catheter. One option to reduce the number of cables is to have the beamforming circuitry external to the body and to use multiplexing on a chip adjacent the array. However, this approach requires use of synthetic-aperture beamforming, which makes the system susceptible to motion artifacts. To prevent this, the data from all of the channels should be processed simultaneously with real-time phased-array beamforming with an integrated circuitry inside the catheter. In that case only one cable is sufficient to transfer the beamformed data. In addition, as discussed in section 1.6, close integration of receive preamplifier electronics with the transducer array

is desired for IVUS systems to improve the system SNR by minimizing the parasitic effects.

In this chapter, realization of an integrated, power-efficient and high-bandwidth current-mode all-pass-filter-based analog delay cell that can generate variable delays at high frequencies is described. This delay circuitry is used as the basic building block in the unit-delay architecture that is discussed in Chapter 6. Design and testing of an analog beamformer IC that is suitable for monolithic integration with the CMUT annular array to implement dynamic receive beamforming is discussed. At the end of the chapter, a method to improve the dynamic range of the developed delay cell is investigated.

7.1. Current-Mode High-Frequency Delay Cell Design

The CMUT annular array targeted in this work operates within a frequency band of 30 MHz to 50 MHz. The delay circuitry should have a flat magnitude response and a constant group delay within this bandwidth of the transducer signal. In addition, it is important that the gain of the delay element is accurately predicted and a gain of 1 per delay stage is a natural choice for a cascade of delay elements.

7.1.1. All-Pass-Based Delay Cell

An ideal delay structure should exhibit a transfer function given by $H(s)=e^{-sTd}$, where Td is the desired delay. However, this exponential transfer function of an ideal delay cannot be realized with a finite number of lumped elements. Instead, an efficient first-order approximation to an ideal delay can be realized using a first-order all-pass

filter. The transfer function of a first-order all-pass filter can be realized by implementing the difference equation that contains a low-pass function as given below

$$\frac{1-s\tau}{1+s\tau} = \frac{2}{1+s\tau} - 1 \tag{60}$$

Based on this expression a current-mode approximation to an all-pass filter can be implemented with the circuit in Figure 92 [204].

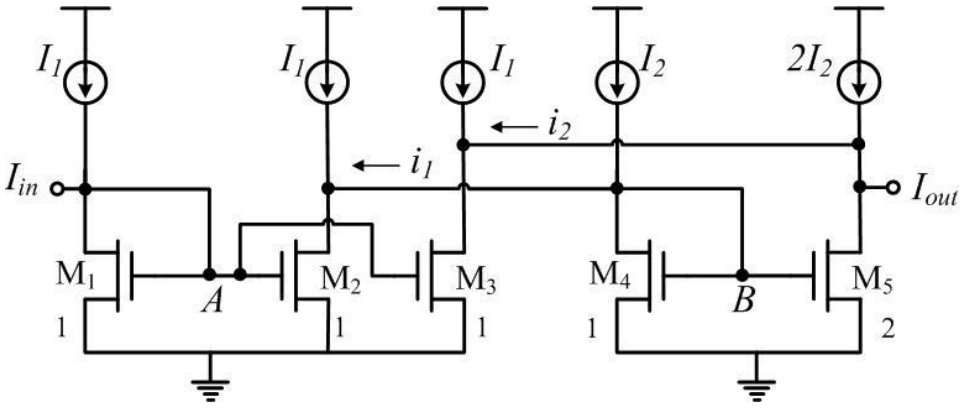


Figure 92. A representative schematic of the all-pass-based delay cell. The "ac small-signal branch currents" are displayed in the figure. The relative sizings of the transistors are also noted.

In this circuit, the input small signal current is mirrored to produce currents i_1 and i_2 through M2 and M3. By selecting $(W/L)_{M5} = 2*(W/L)_{M4}$, the current i_1 is multiplied by 2 through M4-M5 and added to i_2 to produce I_{out}. The resulting current transfer function can be expressed as

$$\begin{aligned} \frac{I_{out}}{I_{in}} &= \frac{-1}{1+sC_A/g_{m1}}\left(\frac{-2}{1+sC_B/g_{m4}}+1\right) \\ &= \frac{1}{1+sC_A/g_{m1}}\frac{1-sC_B/g_{m4}}{1+sC_B/g_{m4}} \end{aligned} \tag{61}$$

where C_A and C_B are the total of the capacitances at the nodes A and B respectively; and g_{m1} and g_{m4} are the small signal transconductance gains of the transistors M1 and M4. As

seen from (61) there is a pole-zero pair associated with node B resulting in the all-pass section in the transfer function. However, the transfer function also includes a low-pass side product due to the pole at the diode-connected node A. To more closely approximate an ideal all-pass filter, the low-pass pole at node A should be pushed to higher frequencies compared to the all-pass pole-zero frequency. In a traditional current mirror, to mitigate the mismatch effects and to keep good current matching, the mirror transistors are forced to have long channels, at least few times the minimum length. This loads the diode-connected node capacitance and limits the bandwidth of the mirror. Furthermore, in this application the delay cells are cascaded shifting the effective 3-dB point to lower frequencies. Therefore, a simple diode-connected current mirror is not sufficient to achieve the required high cut-off frequencies required for this application. Therefore, a bandwidth enhancement technique on the current mirror is necessary.

7.1.2. Broadband Current Mirror

Figure 93 shows a current mirror that is implemented using a current-mode biquad consisting M1 and M2. For stable operation, the second pole at g_{m2}/C_{II} introduced by the source follower buffer (M2) should be placed at a higher frequency compared to the dominant pole at g_{m1}/C_I. If the pole associated with node II (g_{m2}/C_2) is designed to be at a very high frequency, the bandwidth of this biquad mirror is mostly determined by the dominant pole at node I. The source follower feedback (M2) acts as a buffer stage and isolates the input node I and node II. If the gate size of M2 is less than the total size of M1 and M3, than the effective capacitance at the input node reduces. Hence, this biquad mirror exhibits a higher bandwidth compared to a simple diode-connected mirror.

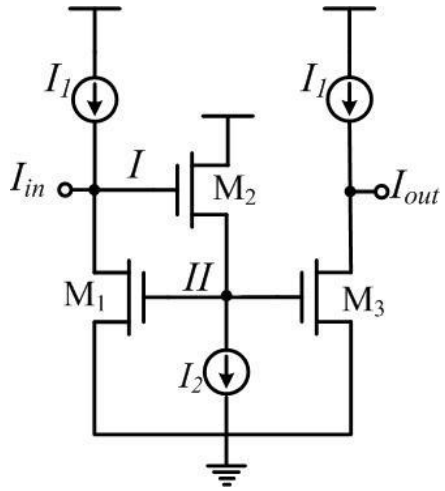


Figure 93. Biquad current mirror

On top of the bandwidth enhancement provided by the node isolation, the bandwidth can be further extended by taking advantage of the fact that a second-order low-pass filter offers a flat amplitude response over a wider range. A small-signal analysis of the two-pole circuit in Figure 93 yields the following current transfer function

$$\frac{I_{out}}{I_{in}} = -\frac{\left(1+s\frac{C_C}{g_{m2}}\right)\frac{g_{m1}}{C_I}\frac{g_{m2}}{C_{II}}}{s^2+s\left(\frac{g_{m2}}{C_{II}}+\frac{1}{r_{o1}C_I}+\frac{1}{r_{o2}C_{II}}\right)+\frac{g_{m1}}{C_I}\frac{g_{m2}}{C_{II}}}, \tag{62}$$

where r_{o1} and r_{o2} are the output resistances of M1 and M2 respectively and g_{m1} and g_{m2} are the transconductances of M1 and M2. C_I and C_{II} are the total of the capacitances at nodes I and II respectively. C_C represents the cross-capacitances between nodes I and II, namely V_{gd} of M1 and V_{gs} of M2. It can be seen that these cross-capacitances introduce a zero in the transfer function but it is at a very high frequency and can be neglected. Assuming r_{o1} and r_{o2} are relatively much higher than $1/g_{m2}$, the transfer function, the peak frequency and the Q of this biquad can be written as

$$\frac{I_{out}}{I_{in}} = -\frac{\frac{g_{m1}}{C_I}\frac{g_{m2}}{C_{II}}}{s^2 + s\frac{g_{m2}}{C_{II}} + \frac{g_{m1}}{C_I}\frac{g_{m2}}{C_{II}}} \tag{63}$$

$$\omega_0 = \sqrt{\frac{g_{m1}}{C_I}\frac{g_{m2}}{C_{II}}} \;\; \& \; Q = \sqrt{\frac{g_{m1}}{C_I}\frac{C_{II}}{g_{m2}}} \quad . \tag{64}$$

It can be seen that after g_{m1} is set to a value by tuning I_1, the quality factor (Q) of the biquad can be fine-tuned with I_2 to any desired value. This flexibility in fine tuning the Q of the biquad can be used to get a second-order maximally-flat Butterworth response which provides a 40% bandwidth enhancement compared to a first-order low pass response. To numerically demonstrate the bandwidth enhancement of the biquad mirror design, the current transfer functions of the simple diode-connected current mirror and the biquad current-mirror shown in Figure 94 are simulated using 0.35-µm CMOS process models. In both cases, the mirror transistors (M1-to-M3) are biased at 80 µA. In the wideband current mirror, the source follower transistor (M4) is biased at 240 µA. In the actual implemented delay circuitry (see Figure 97), the current mirrors are used in a configuration where they are cascoded and where they have two output branches, each with unity gain. Therefore, in this simulation the performance of the mirrors are simulated in the same conditions. The simulation results demonstrate that the biquad current mirror gives a 2.6 times higher bandwidth compared to the regular current mirror (Figure 95).

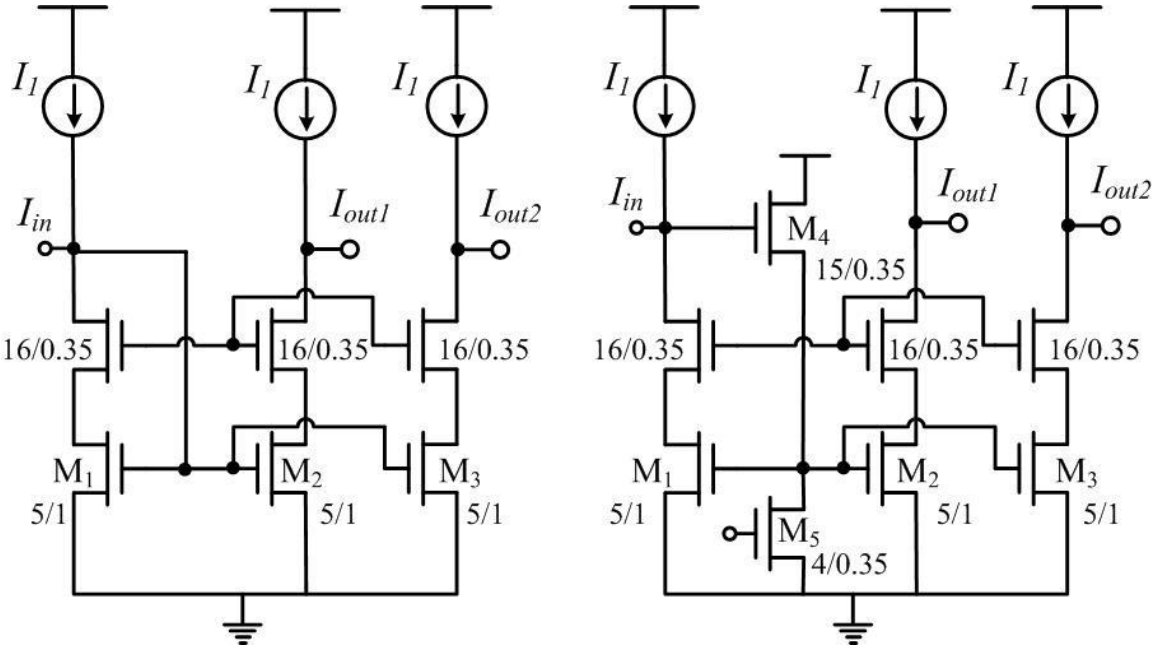


Figure 94. (Left) Simple diode-connected current mirror with two output branches. (Right) Wideband current mirror. Transistor sizes are shown in micrometers.

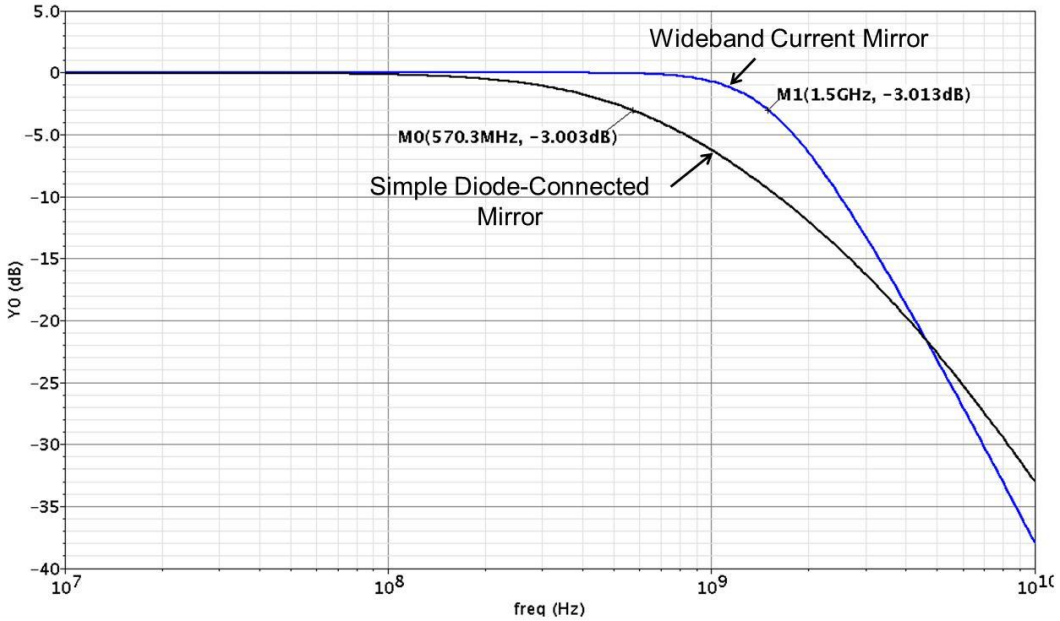


Figure 95. Comparison of the ac response of the simple diode-connected current mirror and the improved wideband current mirror showing the bandwidth enhancement.

In literature, there are some other methods that are proposed for bandwidth enhancement of current mirrors. In [205], to improve the bandwidth of the current mirror, a resistive compensation technique is used where a resistor is placed between the gates of the mirror transistors. One advantage of resistive compensation technique compared to the biquad current mirror design is that the resistive compensation requires smaller voltage headroom. However, its major drawback is the additional thermal noise introduced by the compensation resistor, which results in a significantly higher noise. To improve the noise performance, an inductor can be used instead of a resistor [206]. However, reliable on-chip inductors are hard to get in standard CMOS processes. In the biquad current mirror in Figure 94-right, the primary sources of noise are the current mirror transistors (M1-to-M3). The addition of the source follower (M4) and its bias (M5) does not increase the noise of the mirror significantly. For instance, the current noise of the wideband mirror in Figure 94-right is simulated as 3.83 pA/√Hz which is only slightly higher than the current noise of the diode-connected mirror in Figure 94-left, which is 3.73 pA/√Hz.

It should also be emphasized that in the resistive compensation technique proposed in [205], the maximum increase in the bandwidth is a factor of 2, which happens when the current mirror has unity gain. Otherwise, if the current gain of the current mirror is higher than one, then the increase of the bandwidth becomes less than 2. On the other hand, the bandwidth of the biquad current mirror is not mitigated for current mirrors with a gain higher than unity or for current mirrors with multiple output branches (such as the one used in this work). This is because, thanks to the node isolation,

increasing the capacitive load at node II (see Figure 94-right) does not modify the dominant pole at node I.

7.1.3. Broadband Current-Mode Delay Cell

Figure 96 shows the broadband all-pass delay circuitry, which is an implementation of the current-mode all-pass shown in Figure 92 using biquad current mirrors. The clear motivation to implement the current mirrors containing transistors M1-to-M3 with a biquad mirror is to improve the bandwidth. It can be seen that the current mirror containing M6-M7 pair is also implemented with a biquad approach. A biquad in that mirror is primarily used to keep the drain voltages for nodes A-I and B-I close to minimize the systematic mismatch errors.

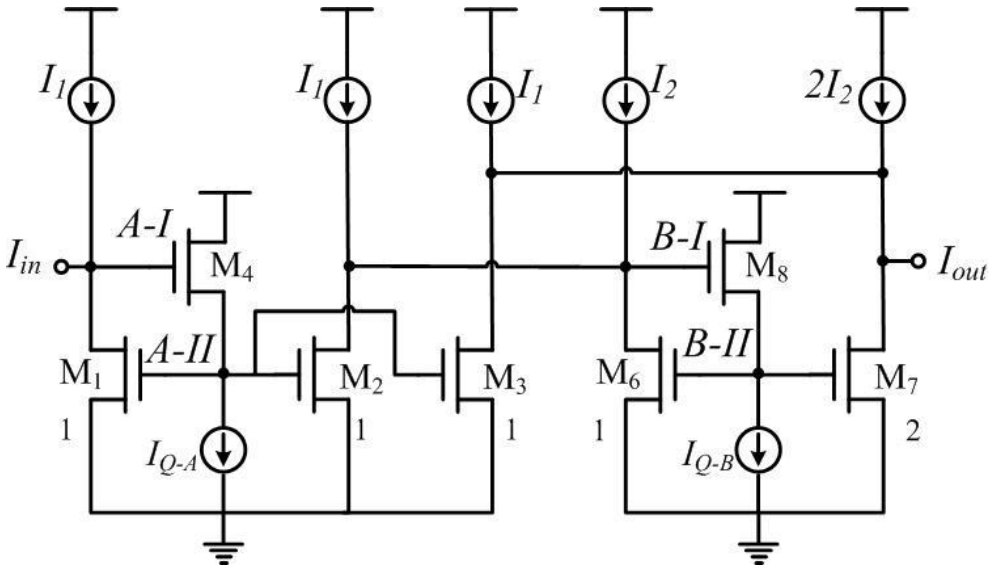


Figure 96. Broadband all-pass filter for delay implementation

The expression for the transfer function of the circuit in Figure 96 is given as

$$\frac{I_{out}}{I_{in}} = H_1 H_2 \tag{65}$$

where

$$H_1 = \frac{\frac{g_{m1}}{C_{A-I}}\frac{g_{m4}}{C_{A-II}}}{s^2 + s\frac{g_{m4}}{C_{A-II}} + \frac{g_{m1}}{C_{A-I}}\frac{g_{m4}}{C_{A-II}}} \tag{66}$$

$$H_2 = \frac{-s^2 - \frac{g_{m8}}{C_{B-II}} + \frac{g_{m6}}{C_{B-I}}\frac{g_{m8}}{C_{B-II}}}{s^2 + \frac{g_{m8}}{C_{B-II}} + \frac{g_{m6}}{C_{B-I}}\frac{g_{m8}}{C_{B-II}}} \tag{67}$$

In this expression, $C_{A\text{-}I}$, $C_{A\text{-}II}$, $C_{B\text{-}I}$ and $C_{B\text{-}II}$ correspond to the total of the capacitances at nodes A-I, A-II, B-I and B-II respectively. It can be seen that H_1 is identical to the biquad low-pass transfer function which was initially shown in (63). On the other hand, H_2 does not correspond to a second-order all-pass transfer function. The magnitude of H_2 is 1 at very low and very high frequencies but at a frequency in between it peaks. Therefore, to prevent peaking in the overall frequency response, it is necessary to push the non-dominant pole (g_{m8}/C_{B-II}) at node B-II to a higher frequency so that the biquad approximates a first-order frequency response with a dominant pole at node B-I. This can be done by keeping the transconductance of M8 high. With a dominant-pole approximation, the overall transfer function of the circuit in Figure 96 can be rewritten as

$$\frac{I_{out}}{I_{in}} = \frac{\frac{g_{m1}}{C_{A-I}}\frac{g_{m4}}{C_{A-II}}}{s^2 + s\frac{g_{m4}}{C_{A-II}} + \frac{g_{m1}}{C_{A-I}}\frac{g_{m4}}{C_{A-II}}} \frac{1 - sC_{B-I}/g_{m6}}{1 + sC_{B-I}/g_{m6}} \tag{68}$$

This expression suggests that the bandwidth of the circuit is controlled by the biquad containing nodes A-I and A-II; and the time constant at node B-I ($C_{B\text{-}I}/g_{m6}$) does not affect the bandwidth.

The total delay of this filter can be discussed in two parts including the delay originating from the low-pass section of the transfer function and the delay of the first-order all-pass part.

The group delay of the first order all-pass part is given as

$$D_{AP}(\omega)=\frac{2C_{B-I}/g_{m6}}{1+\omega^2\left(C_{B-I}/g_{m6}\right)^2}. \tag{69}$$

From this expression, it can be seen that as the frequency increases the filter delay starts to drop from its dc value and therefore, the maximum delay that is constant within a frequency band is limited. This delay dispersion with increasing frequency is common to all continuous-time analog filters and sets a major limitation on the maximum delay that can be implemented using analog filters. The frequency where the delay drops 5% with respect to its dc value is referred as the delay-bandwidth. From (69) it can be seen that the delay-bandwidth is inversely proportional to the dc delay of the filter which depends on the pole-zero frequency of the filter. For instance, the maximum delay, a first order all-pass filter can produce that stays within 5% of its dc value up to 50 MHz frequency is 2.5 ns [124]. Also note that the band where the group delay is relatively constant is much smaller than the pole-zero frequency. For instance when a first-order all-pass filter is tuned to provide a 2.5 ns delay, the pole-zero pair is at 127 MHz, which indicates that the delay-bandwidth (for this case 50 MHz) is around 0.4 times the pole-zero frequency.

The delay of the low pass biquad (the first expression in (68)) can be given as [207]

$$D_{LP}(\omega) = \frac{1}{\omega_0 Q} \frac{1 + (\omega/\omega_0)^2}{\left[1 - (\omega/\omega_0)^2\right]^2 + \omega^2/\left(Q^2 \omega_0{}^2\right)} \tag{70}$$

Considering the expressions for w_0 and Q in (64), the delay at dc, which is equal to $1/w_0Q$, can be found as C_{A-I}/g_{m1}. This indicates that the delay of the low-pass biquad at low frequencies only depends on the current through M1. Fine tuning the Q of the biquad with $I_{Q\text{-}A}$ does not modify the dc value of the delay but only modifies the high frequency behavior of the delay. In our application the discussed low-pass biquad circuit is utilized for its high bandwidth characteristics (i.e. $I_{Q\text{-}A}$ in Figure 96 is fine-tuned to get a Butterworth response). Alternatively if the desired response is to get a constant delay for higher frequencies, Q of the biquad can be configured to implement a linear phase filter (i.e. Bessel-Thomson filter) response which features the maximum delay bandwidth. Therefore, this low-pass biquad circuit is also attractive for implementation of small delays that are constant for higher frequencies. A numerical example can help to clarify this. For instance a first-order low-pass filter can produce 1.25-ns delay that is 5% constant up to 50 MHz; on the other hand a biquad low-pass with Bessel response can generate the same delay while keeping it constant up to 180 MHz.

7.2. Implementation of the Delay Cell in 0.5-µm CMOS

A full transistor implementation of the all-pass-based delay cell (initially shown in Figure 96) in 0.5-µm CMOS is shown in Figure 97. As discussed in the previous section, the poles at nodes A-I ($g_{m1}/C_{A\text{-}I}$) and A-II ($g_{m4}/C_{A\text{-}II}$) determine the behavior of the low-pass section (i.e. bandwidth) of the overall transfer function. Similarly, the pole at node B-I ($g_{m6}/C_{B\text{-}I}$) determine the all-pass behavior (i.e. delay) of the transfer function.

The pole at node B-II ($g_{m8}/C_{B\text{-}II}$) is pushed to a high frequency so it doesn't have a dominant effect. Note that in this particular implementation the current biases through M1-to-M3 and M6-M7 are controlled through a single bias voltage, $V_{Tune\text{-}Delay}$.

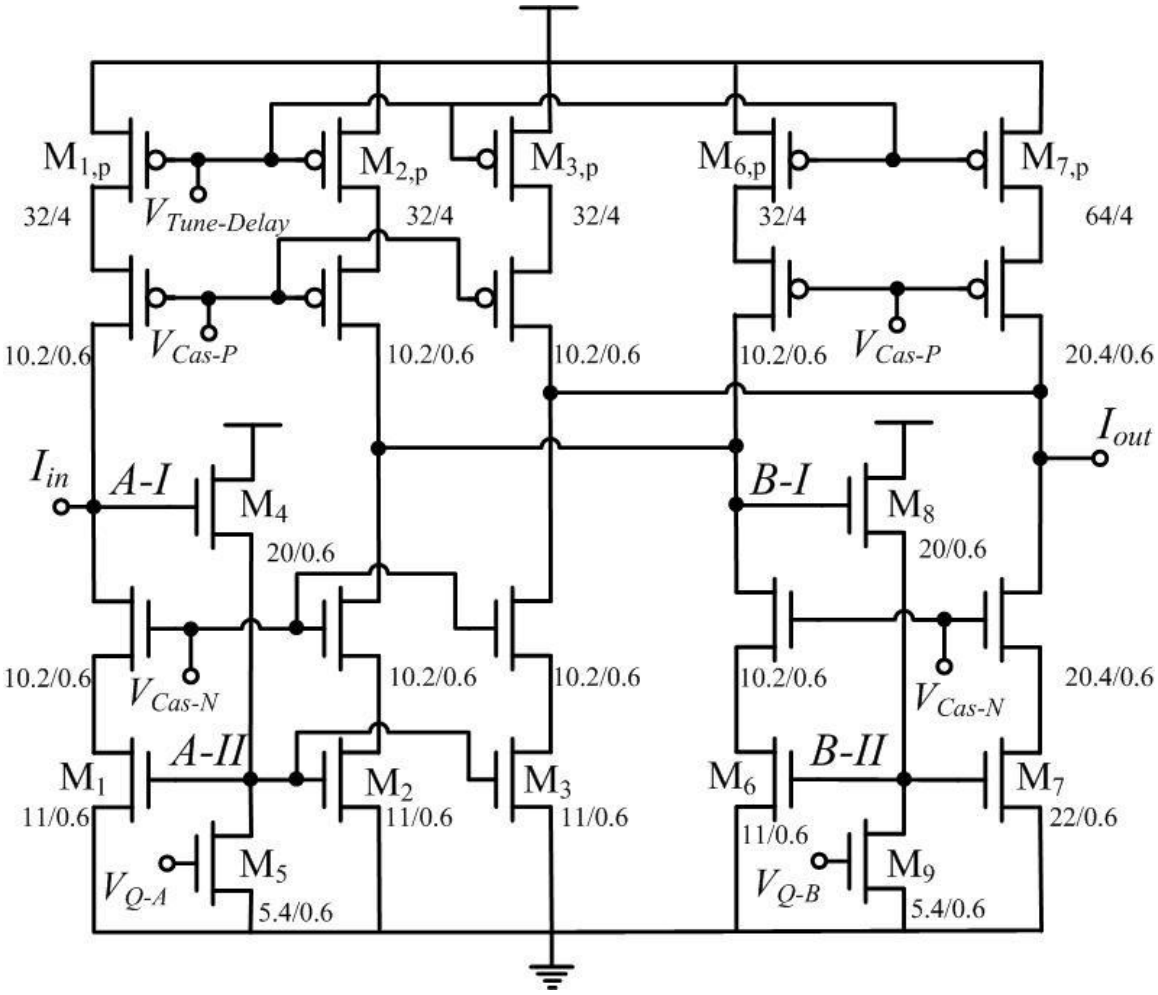


Figure 97. The complete circuit implementation of the proposed analog delay cell in 0.5-μm CMOS. The transistor sizes are given in micrometer.

The minimum delay that the delay cell can provide determines the achievable focusing range since the maximum delay is limited by the maximum allowed delay dispersion along the frequency range and the filter type. In post layout simulations, a 0.95 ns delay is obtained when the delay tuning voltage ($V_{Tune\text{-}Delay}$) is tuned to set the bias

currents to 160 µA. When $V_{Tune\text{-}Delay}$ is tuned to reduce the bias currents to 20 µA, the unit delay increases to 1.7 ns.

Cascoded transistors are used to improve the current transfer accuracy. However, cascoding in the biquad current mirror results in a third pole at the source of the cascode transistors. The NMOS cascode transistors are therefore sized to push the third pole to a very high frequency to neglect the effect of that pole.

The sizes of the PMOS current source transistor (M_{1p}-to-M_{7p}) do not limit the bandwidth since the AC signal doesn't travel through the PMOS transistors unlike the implementation in [204]. Therefore PMOS current source transistors are also sized large with W/L = 32µm / 4µm to have good matched current biases.

To ensure stability, the pole at g_{m4}/C_{A-II} should be higher than the pole at g_{m1}/C_{A-I}. The trade-off in the sizing of the source follower transistor (M4) is that a higher aspect ratio helps to reduce the amount of source follower current needed to achieve a high enough g_{m4} to ensure stability; however a higher aspect ratio also increases the capacitance at node A-I, which reduces the bandwidth. In this design, the W/L ratio of M4 is chosen to be 20 µm/ 0.6 µm. The current value through M8 is set to 160 µm, which is twice the current through M4. This high current through M8 is required to approximate a first order all-pass response for the biquad on node B. In post layout simulations, for low delay setting (0.95-ns unit delay) the power consumption of the delay cell is 7.5 mW through a 5 V supply. For higher delay settings the power consumption reduces. For instance, for 1.7 ns unit delay setting the power consumption becomes 3.3 mW.

Figure 98 shows the micrograph of a beamformer front-end IC that is custom designed and fabricated in a 0.5-µm standard CMOS process. Figure 99 shows the contents of the IC including the delay line based on the unit-delay beamforming architecture, which is discussed in section 6.2. The IC also consists of 8 transimpedance amplifiers, voltage-to-current converters, and two buffers.

This IC is designed to interface with an 8-element annular array with a frequency band between 30 MHz and 50 MHz. CMUT1 in Figure 99 represents the output of the innermost element and CMUT8 represents the output of the outermost element of the annular array. The received signals are amplified and then converted to currents to be added to the delay line. Current-mode delay circuitry enables direct addition of the amplified current signals at the tap nodes.

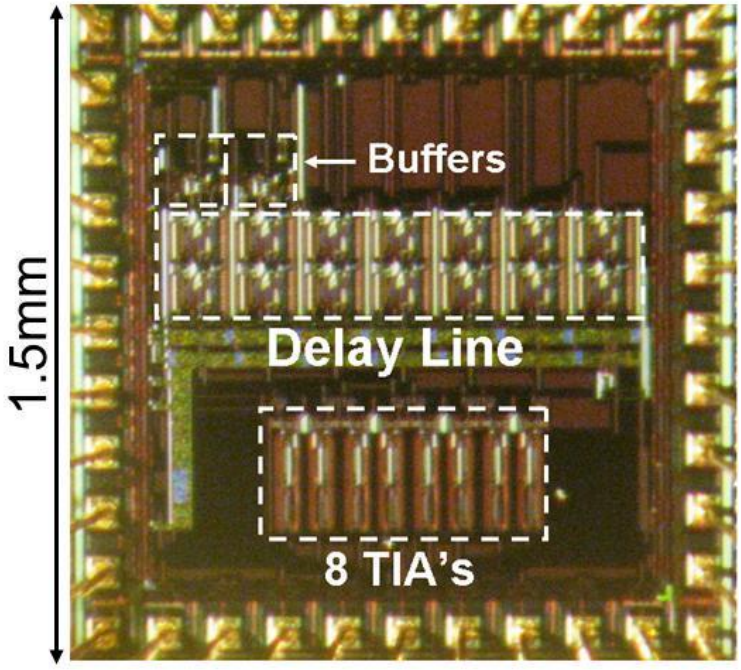


Figure 98. The micrograph of the IC in 0.5-µm CMOS process including preamplifiers (TIAs) and a delay line based on analog delay elements

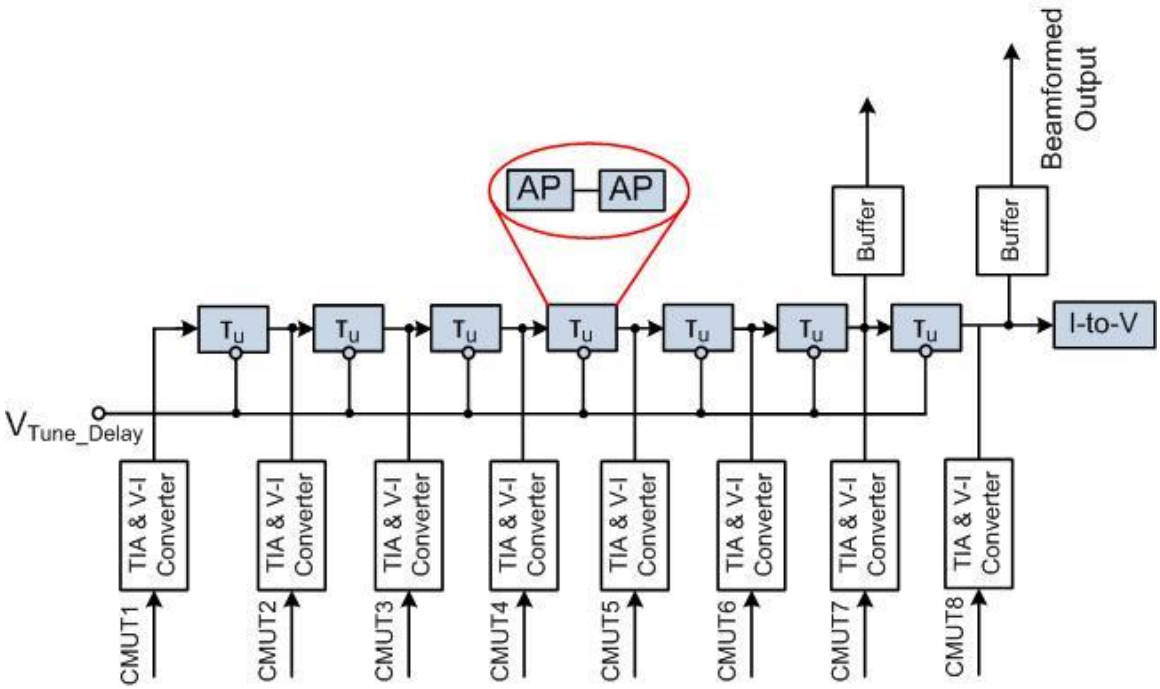


Figure 99. Content schematic of the integrated circuit shown in Figure 98. The focal distance can be varied dynamically by tuning the unit delay (τ_u) value.

In this application, each delay stage between adjacent channels needs to produce delays up to 5 ns (see Figure 91) that are relatively constant up to 50 MHz range. The delay cell used in the delay line is based on the discussed current-mode all-pass filter shown in Figure 97 and as discussed earlier, a single all-pass filter stage cannot provide the required 5-ns stage delay. Therefore each delay stage is composed of 2 delay cells as shown in Figure 99. The delay line contains 7 stages and a total of 14 all-pass-based delay cells. All identical delay cells are controlled and tuned simultaneously through one external control voltage (V_{Tune_Delay} in Figure 97 and Figure 99).

Since the delay cells are cascaded, the output dc voltage of the previous cell is determined by the input dc voltage of the following cell. An I-to-V stage is included to set the dc bias voltage for the last delay cell. This I-to-V stage is identical to the low-pass

section of the circuit that includes M_1-M_3 and M_{1p}-M_{3p} in Figure 97. Note that there are no high impedance nodes throughout the delay line.

For this current-mode approach, it is critical to have good current matching. Therefore a finger symmetrical structure is employed in the layouts of the current mirrors of the delay cell to improve the device matching. Each designed delay cell in the delay line consumes a 125 μm x 150 μm chip area.

The particular IC that is shown in Figure 98 uses a delay cell where $V_{Q\text{-}A}$ and $V_{Q\text{-}B}$ (see Figure 97) are tied together. There is another version of this IC where $V_{Q\text{-}A}$ and $V_{Q\text{-}B}$ are separated in the used delay cells (the exact circuit shown in Figure 97). The electrical measurements of the delay line that are presented in the following section are obtained from that design where $V_{Q\text{-}A}$ and $V_{Q\text{-}B}$ are separated.

7.2.1. Electrical Characterization

Although the delay circuitry is in current mode, it can be tested with voltage-mode input and output. The applied voltage is converted to a current with the input resistance of the current mirror and again converted to a voltage at the last I-to-V stage. For the below measurements, the input of the first delay stage is directly connected to a 4395A Agilent spectrum-network analyzer using a switch that bypasses the amplifier and the V-I converter. The output is taken after 7 delay stages from the last buffer output shown in Figure 99.

Cascaded delay of the 14 delay cells in the delay line is measured at different delay tuning voltages (Figure 100). It can be seen that each delay cell can generate delays

between 1.25 ns to 2.45 ns and the delays are relatively constant within the frequency band.

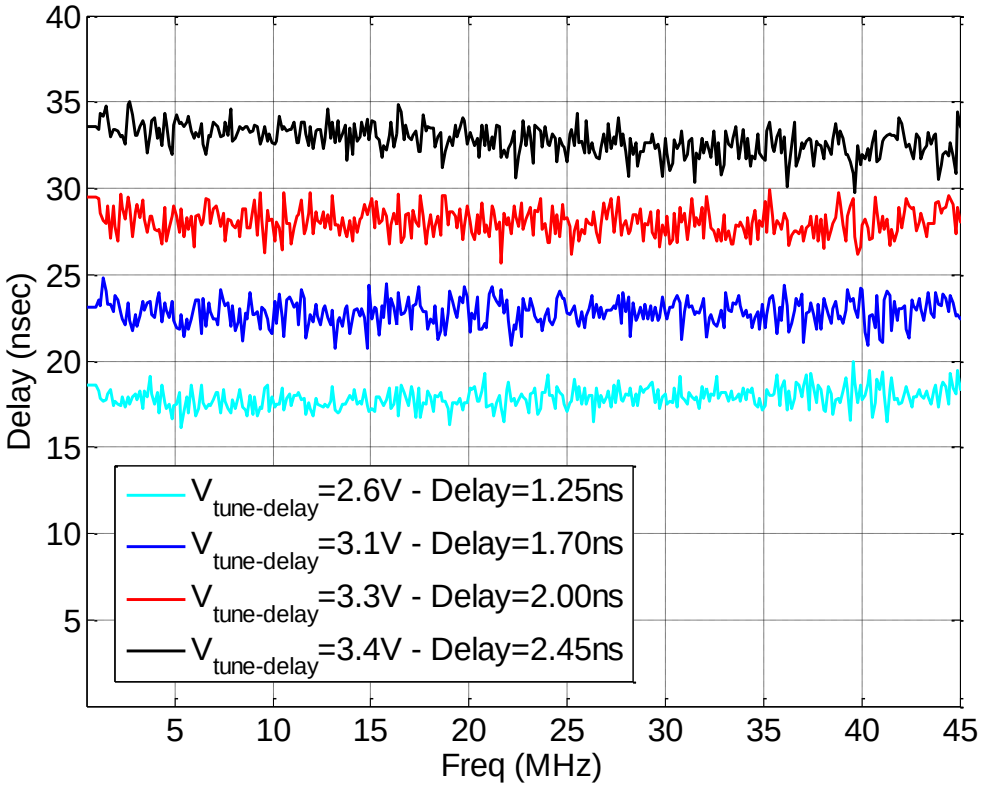


Figure 100. Delay of 14 cascaded delay cells for different delay tuning voltages. This measurement indicates that each delay cell can generate delays between 1.25 ns to 2.45 ns

Figure 101 shows the frequency response of the cascaded 14 delay cells at different delay settings. The plotted gains are corrected for the gain loss of the output buffer and the gain for the low delay setting is normalized to one. It can be seen that for higher delay settings the bandwidth of the delay line reduces. This is because the bias current through M1, which determines the low-pass pole, is also reduced to increase the delay. Nevertheless, even for the 2.45-ns unit delay setting, the signal bandwidth of 14

delay cells is measured to be higher than 50 MHz, suitable for a 30 MHz to 50 MHz annular array.

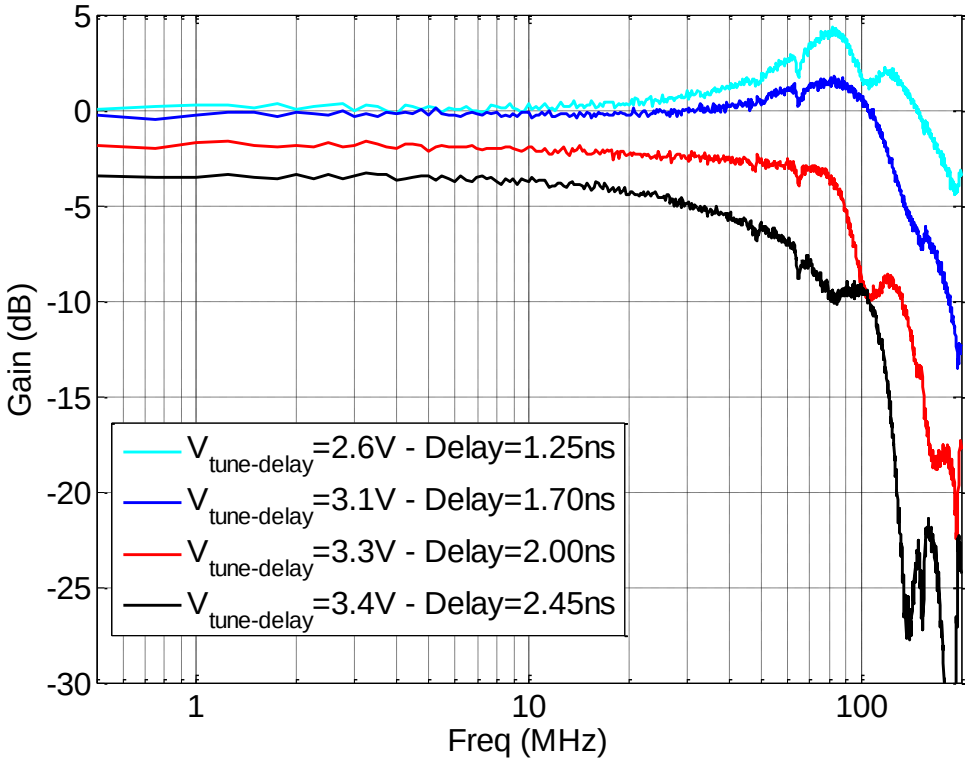


Figure 101. Gain measurement of 14 cascaded delay cells

Table 10 contains the post layout simulated and measured values for the delay of a single delay cell along with the bandwidth and dynamic range of the delay line containing 14 delay cells. For the delay of a single cell, the pre-layout simulated values are also included to highlight the fact that the pre-layout simulated delay values are considerably smaller than the measured delay values. This shows that the layout parasitics has a substantial effect and should be considered during the design stage. The layout extraction tool that was available at the time of the design of this IC only extracted parasitic capacitances. Therefore the post layout simulations do not incorporate the

parasitics for the routing metal sheet resistances. Thus, it is expected that the measured results depict a higher delay than the post layout simulations since the parasitic resistors were not accounted for in the post layout simulations.

Table 10. Simulated and measured characteristics of a delay line including 14 delay cells

		Voltage Settings	Delay of a single cell (ns)	BW of 14 cascaded delay cells (MHz)	Dynamic Range of the delay line (dB)
Low Delay Setting	Post layout Simulation	$V_{Tune\text{-}Delay}$ = 2.8V; $V_{Q\text{-}A}$ = 1.5V $V_{Q\text{-}B}$ = 2.0V	0.65 (Pre layout) 0.95 (Post layout)	98	53
	Measurement	$V_{Tune\text{-}Delay}$ = 2.6V; $V_{Q\text{-}A}$ = 1.5V $V_{Q\text{-}B}$ = 2.0V	1.25	180	51
High Delay Setting	Post layout Simulation	$V_{Tune\text{-}Delay}$ = 3.6V; $V_{Q\text{-}A}$ = 1.5V $V_{Q\text{-}B}$ = 2.0V	1.15 (Pre layout) 1.7 (Post layout)	59	38
	Measurement	$V_{Tune\text{-}Delay}$ = 3.3V; $V_{Q\text{-}A}$ = 1.5V $V_{Q\text{-}B}$ = 2.0V	2.0	80	36
	Measurement	$V_{Tune\text{-}Delay}$ = 3.4V; $V_{Q\text{-}A}$ = 1.5V $V_{Q\text{-}B}$ = 2.0V	2.45	60	30

In the gain measurements in Figure 101 there is a slight peaking for low delay settings, which is probably the reason for the measured bandwidths being higher than the simulated ones that are shown in Table 10. This peaking is believed to be caused by the third pole at the source of the cascode in the biquad and does not introduce any unstability concerns. Nevertheless, in the next generation design in 0.35-μm CMOS, to prevent that peaking, the aspect ratio of the NMOS cascode transistors are increased (see Figure 107) to push that third pole to higher frequencies.

For higher delay settings (smaller bias currents) the dynamic range reduces and drops to 30 dB for 2.45 ns delay setting (Table 10). This is a drawback of tuning the delay through the bias current. Therefore, in this case the maximum delay value is not limited by the delay dispersion but actually is limited by the required dynamic range.

7.2.2. Receive Beamforming Experiment with CMUT Annular Array

To test the beamforming capability of the fabricated IC, an 8-element 840-μm diameter CMUT annular array was integrated with the IC using cable connection. For receive beamforming characterization, the outermost element of an identical annular array which is an 18-μm wide ring is imaged. The transmitter element was placed 3.2 mm away from the beamformed receiver array and 4 cycles of a 38 MHz bipolar pulse was transmitted (Figure 102). All 8 elements of the annular array were connected to the delay line IC. The radiated field was scanned with the receiver array and at each step of the scan the beamformed signal is collected with three different delay tuning voltages that focus the receiver array to 1.6 mm, 2.5 mm and 3.2 mm. Figure 103 presents the normalized beamformed signal amplitude as a function of lateral position for receive focal points set at 1.6 mm, 2.5 mm and 3.2 mm imaging the 18-μm target, which was located 3.2 mm away. The functionality of receive beamforming is validated by a side lobe reduction of ~10 dB when the receive focal point is set to 3.2 mm, which corresponds to the distance of the target.

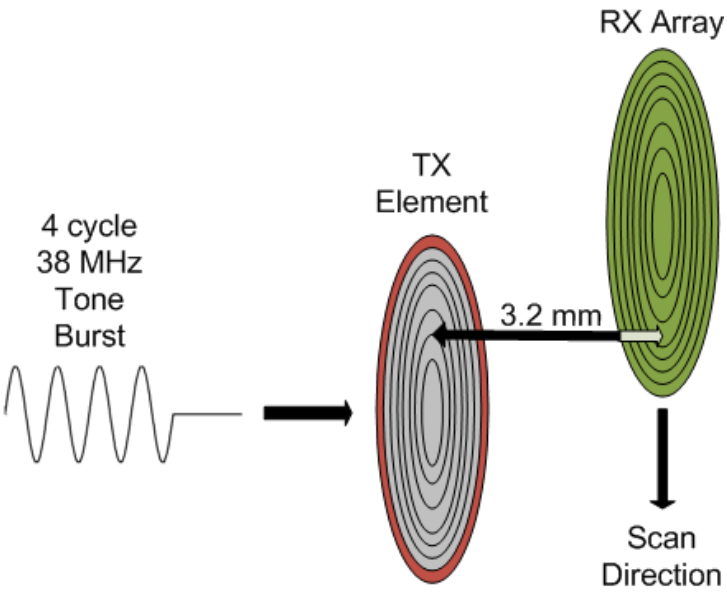


Figure 102. Test setup for receive beamforming characterization

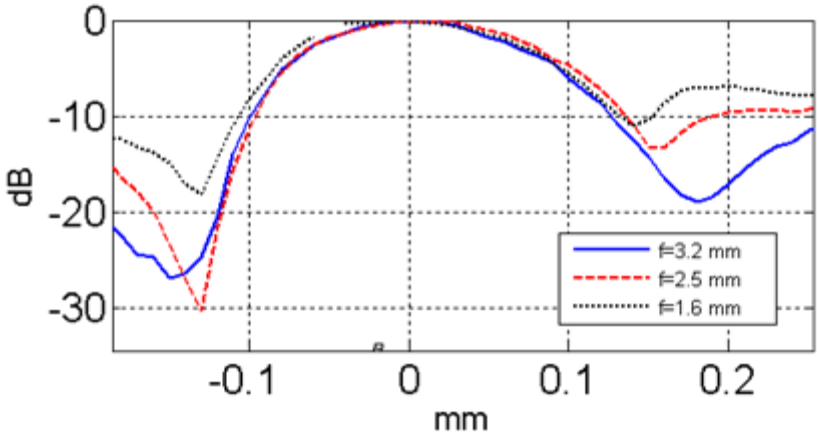


Figure 103. Cross-sectional image of the 18-μm transmitting ring (at 3.2-mm distance from the receive ring) for receive focal points tuned for 3.2 mm, 2.5 mm and 1.6 mm.

7.3. Receive Beamformer IC for Monolithic Integration with the CMUT Array

As discussed earlier, single chip integration is desired for implementation of compact and high-performance IVUS probes. Figure 104 illustrates a side-looking IVUS probe for high-frequency (30-50 MHz) ultrasound imaging. It can be seen that the probe

architecture includes a beamformer IC that is monolithically integrated with the annular array.

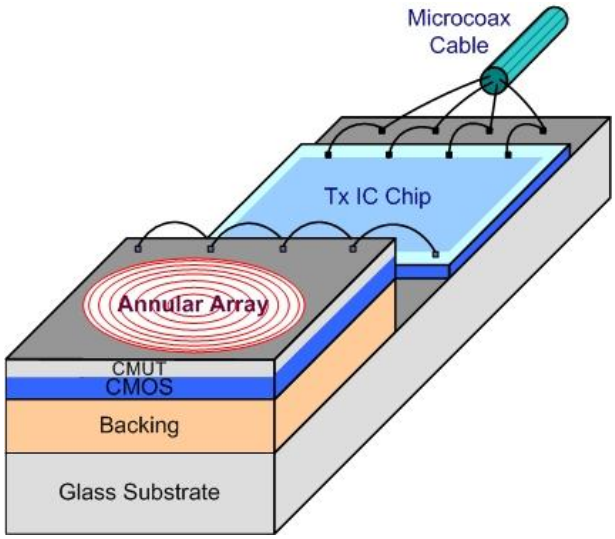


Figure 104. SL-IVUS probe architecture where the receiver IC and the CMUT array are monolithically integrated. The TX IC is shown to be separately connected.

The beamformer IC discussed in the previous section was designed for initial characterization and verification of the beamforming approach before attempting the design of a beamformer IC suitable for monolithic integration with the transducer array. Based on the design approaches developed with that 0.5-µm CMOS chip, a dynamic receive beamformer IC is designed and fabricated in 0.35-µm two-poly, four-metal CMOS technology (the wafer run discussed in section 4.1). The chip is suitable for single-chip integration with a 1.6-mm diameter 16-element annular array. Figure 105-top shows the micrograph of the fabricated chip. Each delay cell occupies an 80×100 μm^2 area. The chip is 2 mm x 2 mm in size but the total active area of the amplifiers, delay line and the buffers is only 1.2 mm x 0.3 mm. This area consumption is small enough to easily fit under the 1.6-mm diameter annular array.

The beamformer IC is capable of buffering, delaying and preamplification for 8 receive channels. The other 8 elements in the 16-element array are reserved for transmit operation. Therefore, no transmit receive switch is included in this particular IC implementation. This beamformer chip does not incorporate high voltage pulsers. However, note that if desired both the transmit pulsers and transmit-receive switches can easily be incorporated in the future designs to enable 16 element single chip receive and transmit operation.

Figure 105-bottom shows a representative illustration that shows how the single-chip integrated system would look like after the CMUT array is monolithically integrated with the IC. The connections between the CMUT array and the CMOS IC will be done through the metal stacks located horizontally on the center of the IC. In addition to the earlier discussed advantages of monolithic integration (i.e. reduced interconnect complexity and interconnect parasitics) this application benefits from another advantage of CMUT-on-CMOS integration. Typically, in an annular array some area is reserved to provide electrical connections to the center transducer elements (see Figure 18). This results in loss of active area and asymmetries in the generated beam. CMUT-on-CMOS approach enables to route the required CMUT connections through the CMOS chip which enables to fully utilize the area on the CMUT level. The 8 transmit connections routed through the CMOS chip to the output pads on the bottom of the IC can be seen in the chip micrograph in Figure 105-top.

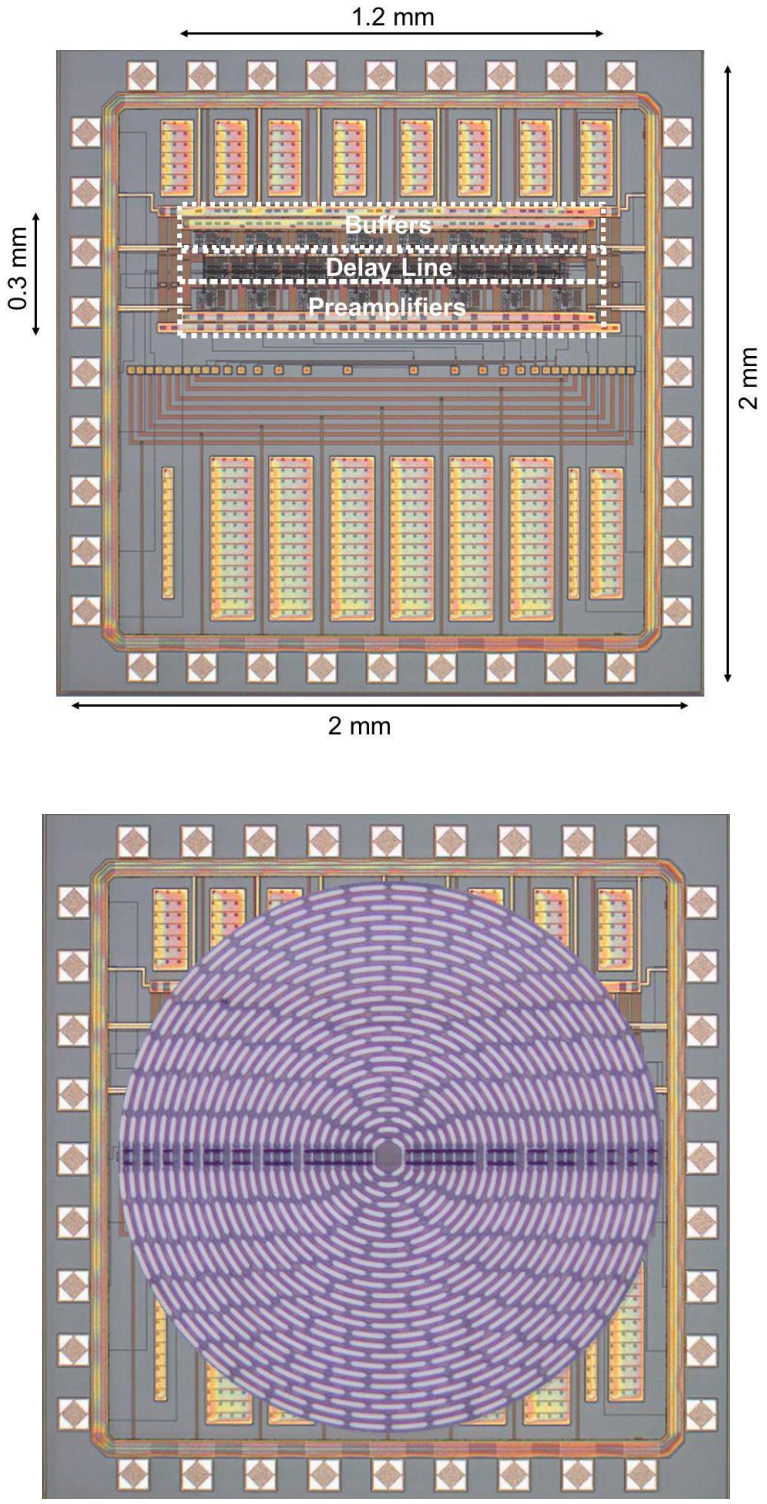


Figure 105. (Top) The micrograph of the beamformer IC designed to interface with a 1.6-mm diameter annular array. (Bottom) Representative figure of how the chip will look like after the CMUT array gets monolithically integrated with the CMOS chip.

Figure 106 shows the content schematic of the IC, which includes 8 receive amplifiers, a delay line and 8 separate buffers connected to each node of the delay line. Each delay stage is composed of 2 all-pass-filter-based delay cells. All identical delays are controlled and tuned through one external control voltage simultaneously. Even though one buffer would suffice to get the beamformed data, for testing purposes a buffer is connected to each tap. It is not explicitly shown in Figure 106 but each buffer is connected to the delay line through a very small-sized source follower. This minimizes the capacitive loading of the buffers to the delay line. In this IC, the transimpedance amplifier followed by the voltage-to-current inverter scheme, which was used in the 0.5-µm chip (see Figure 99), is replaced by a current preamplifier. This change is motivated by the fact that since the delay circuitry is current based and the CMUT signal is in currents; a current preamplifier is better suited for this beamforming application.

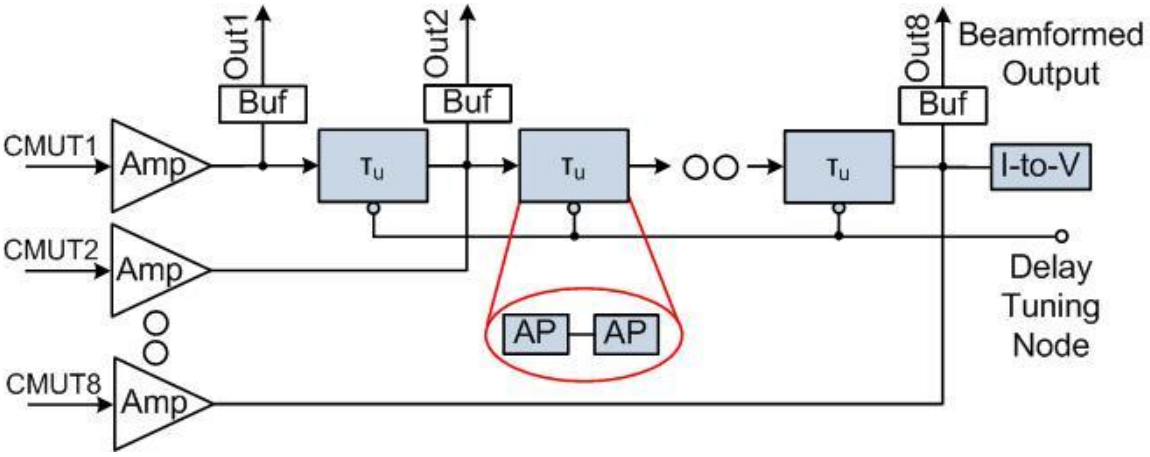


Figure 106. Content schematic of the beamformer IC. Each delay stage consists of two analog delay cells and there are total of 14 delay cells on the delay line.

7.3.1. Delay Cell

Figure 107 shows the schematic of the implemented delay cell. This delay cell version features some changes compared to the initial 0.5-µm design shown in Figure 97. In the 0.5-µm design, the delay control voltage also controlled the bias current through M1 and the bandwidth of the filter dropped for higher delay values (as seen in Figure 101). In this delay cell design, the delay control voltage ($V_{Tune\text{-}Delay}$) and the voltage that control the bias current through M1 (V_{Bias}) are separated, which enables to tune the delay without limiting the bandwidth. In addition, the smaller node technology enables to reduce the power consumption of the delay circuitry. Each delay cell in this IC consumes a 2.1-mW peak power (at low delay setting), which is relatively lower compared to the 7.5-mW peak power consumption of the delay cell designed in 0.5-µm CMOS.

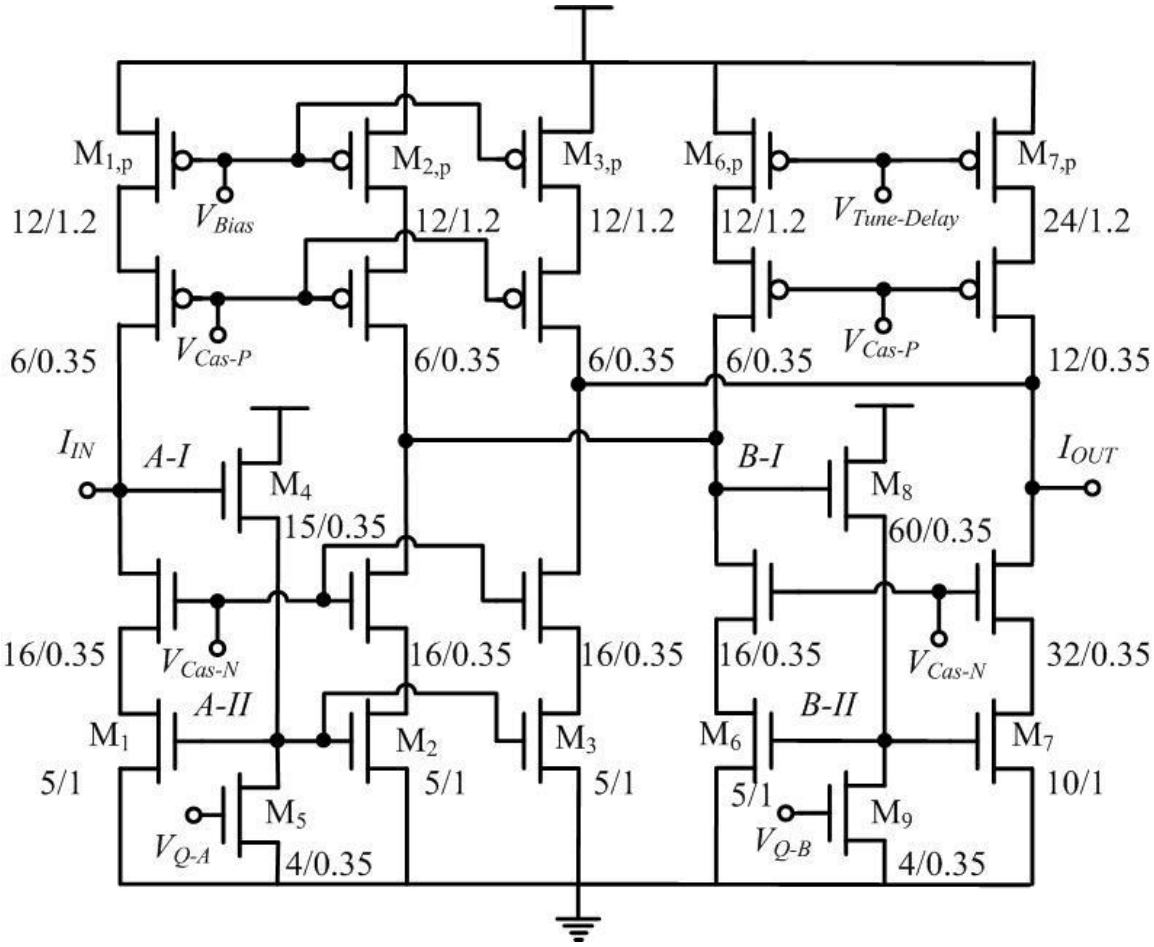


Figure 107. The complete circuit of the proposed all-pass filter-based analog delay cell with the transistor sizes shown in micrometers.

The sizing of the current mirror transistors (M1-to-M3 and M6-M7) is one of the most critical design choices in the design of the delay cell. The sizing is subject to various trade-offs between the minimum delay, bandwidth, current mirroring accuracy and power consumption. These trade-offs are discussed in the following two paragraphs. Before that discussion though, it should be reemphasized that the pole at $g_{m1}/C_{A\text{-}I}$ mostly determines the bandwidth and the dc delay of the all-pass section is mostly determined by and is inversely proportional with the pole at $g_{m6}/C_{B\text{-}I}$.

In a traditional diode-connected current mirror, when the width of the current mirror transistors is increased the transconductance improves but the bandwidth of the mirror does not necessarily improve because increasing the sizes of the transistors also increases the capacitance at the diode-connected node. In that regard, an important advantage of the biquad current mirror design is that its node isolation feature enables to increase the sizes of the current mirror transistors (M1-to-M3 in Figure 107) without loading the capacitance at $C_{A\text{-}I}$. This enables to improve the bandwidth by increasing the width (and hence g_{m1}) of the mirror transistors. In addition, the need for a high output resistance for better current mirroring accuracy requires the gate lengths of the NMOS current mirror transistors (M1-to-M3 and M6-M7) to be few times higher than the minimum length. In a traditional diode-connected current mirror increasing the length of the transistors would also increase the capacitance loading and hence would reduce the bandwidth. However, with the biquad design, again thanks to the node isolation, the current mirror lengths can be increased to improve matching without the bandwidth tradeoff.

Similarly, the node-isolation of the biquad mirror design also enables to decrease the minimum delay by increasing the sizing of the current mirror transistors (M6-M7) to increase g_{m6}, without increasing $C_{B\text{-}I}$. On the other hand, it should be mentioned that in the biquad design the sizes of the current mirror transistors cannot be increased indefinitely. With increased transistor sizes, the capacitance at the gates of the mirror transistors ($C_{A\text{-}II}$ and $C_{B\text{-}II}$ in Figure 107) also increases. With increased capacitances at $C_{A\text{-}II}$ and $C_{B\text{-}II}$, to ensure stability the required currents through the source followers (M4 and M8) also need to be increased, which in turn increases the power consumption. In

addition, the increased size of the current mirror transistors reduces the third pole frequency on the drain of the mirror transistors, which is not desired. Considering all these effects, in this design a 5µm/1µm aspect ratio (M1-to-M3 and M6) is chosen as a good midpoint between the minimum delay, bandwidth, power consumption and current matching requirements. The width of M7 is sized as 10 µm, twice the size of the M6, as required by the architecture.

In simulations, the broadband current mirror that contains the nodes A-I and A-II is shown to enhance the bandwidth around 3 times compared to a simple diode-connected current mirror. Some of the bandwidth improvement comes from the node isolation, and the rest is achieved when the current through M4 is tuned to obtain a 2^{nd}-order Butterworth response. Also note that, in this application 14 of these delay cells are cascaded. When 14 first-order low-pass filters are cascaded, the overall 3-dB frequency becomes 0.225 times the 3-dB of a single low-pass filter. On the other hand, cascading 2^{nd}-order Butterworth low-pass filters results in only a 0.48 times bandwidth reduction. Therefore, having Butterworth response provides further 2.13 times improvement over cascading first-order low-pass filters. When these effects are combined, in this application, the overall bandwidth improvement of the broadband current mirror becomes approximately 6 times.

As discussed earlier the biquad that contains nodes B-I and B-II should be approximated as a first-order response to prevent peaking in the gain response. A high g_m on the source follower (M8) helps to push the secondary pole in the biquad to higher frequencies. Therefore, M8 is sized with a relatively large aspect ratio of 60 µm/0.35 µm which is 4 times the size of M4.

Figure 108 plots the simulated delay of the delay cell for two different delay control voltages. A minimum delay of 1.1 ns is obtained when V_{Bias} and $V_{Tune\text{-}Delay}$ are tuned to the same voltage to set the bias currents to 80 μA. The total delay can be tuned up to 2.5 ns by keeping the bias current through M1-to-M3 at 80 μA and by reducing the bias current through M6, which tunes the delay, to 10 μA.

The expression for the total delay of the delay cell can be written by combining the expressions in (69) and (70) into a single equation:

$$\begin{aligned} D(\omega) &= D_{LP}(\omega) + D_{AP}(\omega) \\ &= \frac{C_{A-I}}{g_{m1}} \frac{1+(\omega/\omega_0)^2}{\left[1-(\omega/\omega_0)^2\right]^2 + \omega^2/\left(Q^2\omega_0{}^2\right)} + \frac{2C_{B-I}}{g_{m6}} \frac{1}{1+\omega^2\left(C_{B-I}/g_{m6}\right)^2} \end{aligned} \tag{71}$$

where

$$\omega_0 = \sqrt{\frac{g_{m1}}{C_{A-I}} \frac{g_{m4}}{C_{A-II}}} \;\; \& \; Q = \sqrt{\frac{g_{m1}}{C_{A-I}} \frac{C_{A-II}}{g_{m4}}} \tag{72}$$

The delay contribution of the low-pass section of the transfer function is also plotted in Figure 108 with a dashed line. Note that this corresponds to the frequency shape of the first expression in (71). The low-pass section delay shows a little peaking at high frequencies because the biquad is tuned for a Butterworth response. However, the delay contribution of the all-pass section rolls off at those frequencies so the total filter delay does not peak. The low-pass section of the transfer function accounts for only 0.25-ns of the total filter delay and the delay contribution of the all-pass section dominates over the delay contribution of the low-pass part. This is because the large aspect ratio of M8 increases the capacitance at node B-I compared to the total capacitance at node A-I. Therefore, even when the current biases are the same, the low pass pole at g_{m6}/C_{B-I} is at a relatively higher frequency compared to the all-pass pole-zero pair at g_{m1}/C_{A-I}.

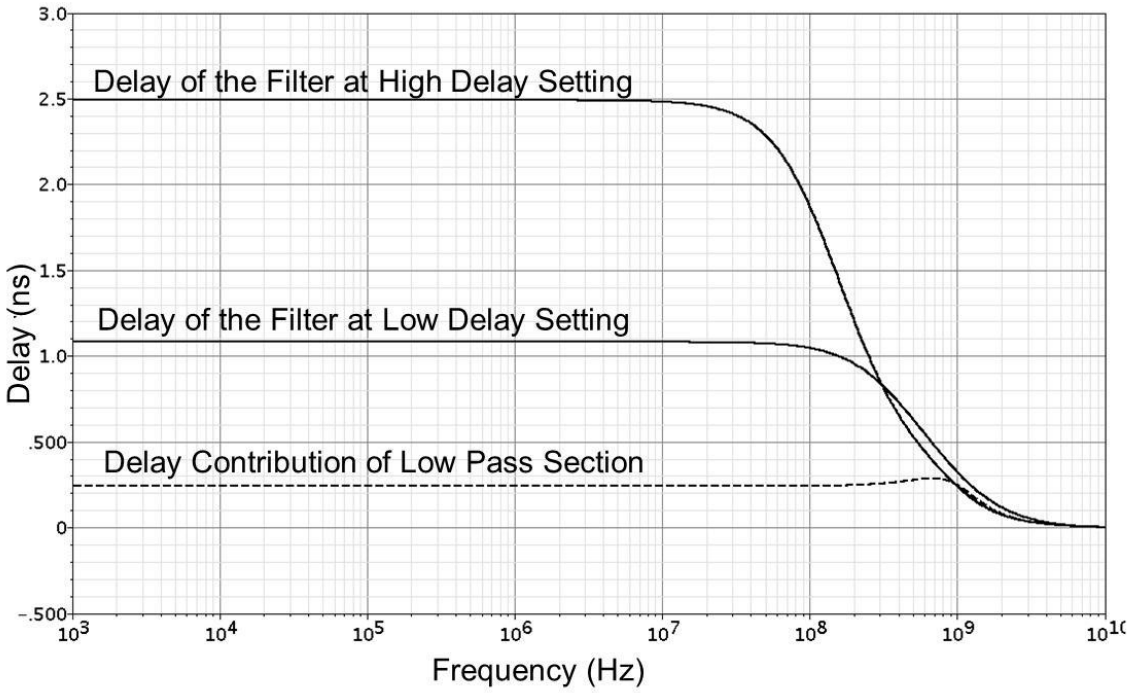


Figure 108. Simulated delay with different delay tuning voltages. Delay can be tuned between 1.1 ns and 2.5 ns.

7.3.2. Electrical Characterization of the Delay Cell

For the electrical characterizations, the active contents of the beamformer IC are included in a test chip. In this test chip the amplifier inputs are routed to pads, unlike the CMUT-on-CMOS IC shown in Figure 105 where the amplifier inputs are directly connected to the CMUT elements. For the gain measurements, two outputs of the IC at taps 1 and 8 (see Figure 106) are connected to two ports of an Agilent 4395A network analyzer. Figure 109 shows the measured cascaded gain of 14 delay cells adjusted for 2-ns delay. It can be seen that the bandwidth is improved from 60 MHz to 150 MHz by tuning the Q control ($V_{Q\text{-}A}$) of the low-pass biquad. In this case the measured 150-MHz bandwidth is 3 times higher than 50 MHz, which is the upper frequency limit of the transducer signal. Having a high bandwidth in the delay line is advantageous for several

reasons. The first advantage stems from the fact that the overall bandwidth of the receive signal chain gets also reduced by the bandwidth of the preamplifier. For instance, if the delay line bandwidth is 80 MHz then the preamplifier bandwidth should also be at least 80 MHz to get an overall cascaded bandwidth higher than 50 MHz. This requires a 60% increase on the bandwidth requirement of the preamplifier which necessitates some sacrifice on the gain and noise performance of the preamplifier. On the other hand with a 150-MHz delay line bandwidth, the preamplifier bandwidth can be kept relatively close to 50 MHz. Secondly, in future. if the transducer technology develops to enable higher frequency operation, with its high cascaded bandwidth this delay line will be able to handle those higher frequencies.

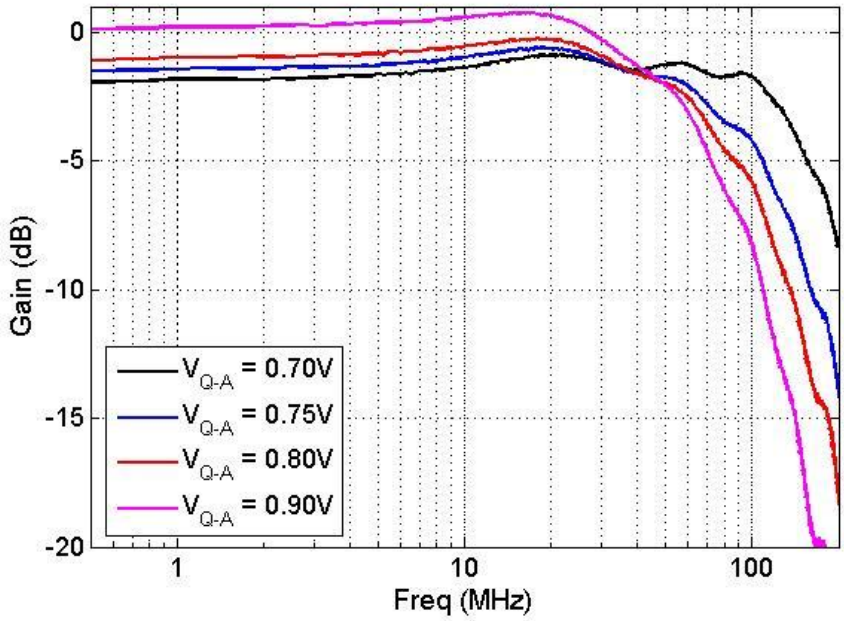


Figure 109. Measured gain of 14 cascaded delay cells with different Q control voltages. Bandwidth improves when the Q control current is reduced in the biquad current mirror to get close to Butterworth response.

Figure 110 shows the gain of 14 cascaded delay cells with different delay tuning voltages. It can be seen that, as expected by the all-pass-based design, for higher delay settings the bandwidth does not degrade. The measured gain of an individual delay cell is -0.34 dB (-4.7 dB for 14 cascaded cells) and -0.14 dB (-2.0 dB for 14 cascaded cells) for 1.75-ns and 2.5-ns delay settings, respectively.

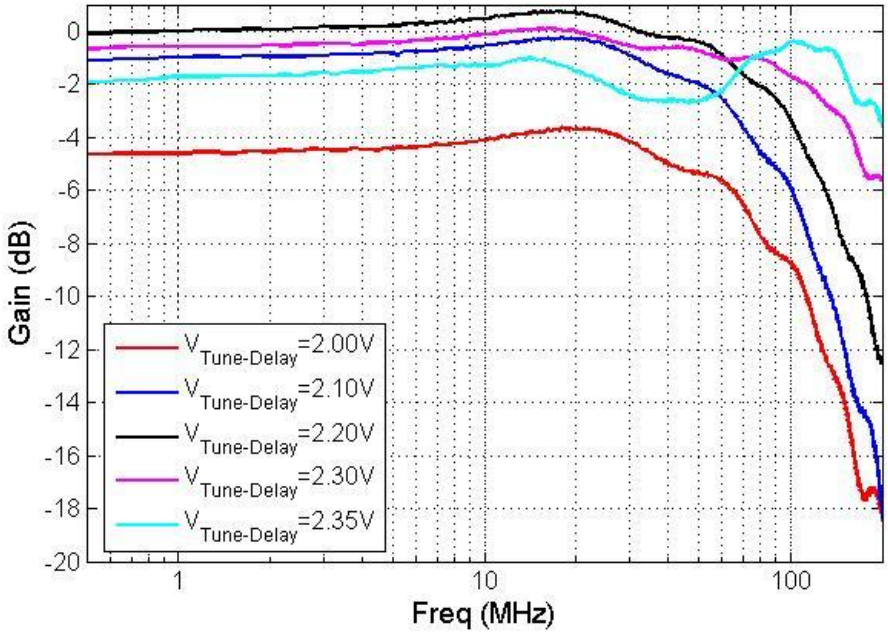


Figure 110. Gain with different delay tuning voltages. The bandwidth does not degrade for higher delay settings. Stage gain stays within -0.34 dB (0.96) for all delay settings.

Figure 111 shows the measured group delay of the consecutive delay stages. The delay cell is tuned for a 2-ns delay for this measurement. The waviness in the measurement is probably due to the cross-coupling of the output signals in the test environment. It can be seen that the delay difference between consecutive stages is similar.

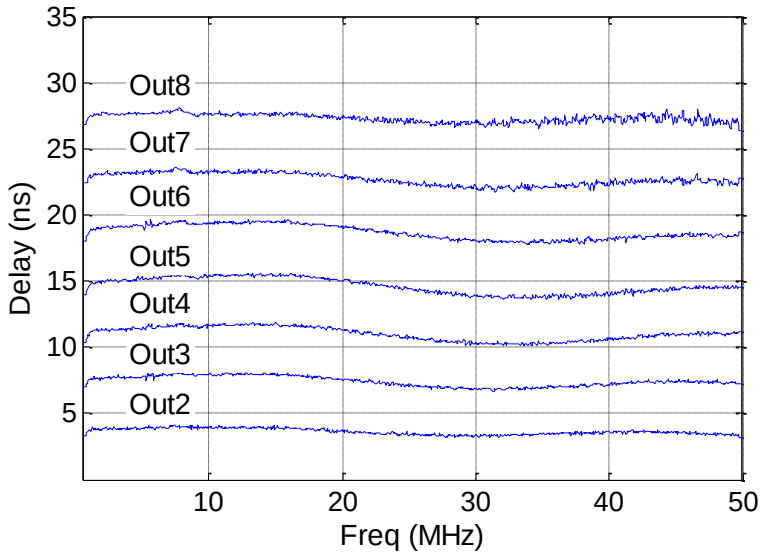


Figure 111. The measured group delay at each tap at a unit delay of 2 ns.

The measured minimum delay of the delay cell is 1.75 ns which is higher than the pre-layout simulated value of 1.1 ns (see Figure 108). The delay increase in the measured results is due to the parasitic loading of the layout routing resistance and capacitances. Accurate post layout extraction models were not available during the design phase therefore post layout simulations could not be performed. Since in this design the total delay is dominated by the delay of the all-pass section of the filter transfer function, the maximum total delay per delay cell, which is limited by the delay dispersion of the all-pass section, is 2.5 ns for 50-MHz operation. In future designs, the delay range can be improved by reducing the minimum delay by increasing the aspect ratio of the transistors M1-M3 & M6-M7 in Figure 107. This can be done by slightly reducing the length of the transistors. As mentioned earlier this won't reduce the bandwidth thanks to the node isolation of the biquad mirror design but can slightly degrade the current matching between the mirrors.

Assuming a transducer signal bandwidth of 20 MHz, the measured dynamic range of one delay cell and the whole delay line at a unit delay of 1.75 ns are 54 dB and 42 dB, respectively. The dynamic range of the delay line reduces to 32 dB at a delay of 2.5 ns because of the reduced bias current through M6 and M7 in Figure 107. A capacitive delay tuning method to eliminate this dynamic range limitation is discussed in section 7.4.

Each delay cell consumes 2.1 mW from a 3.3-V supply at 1.75-ns delay setting. The power consumption of the delay line and a single buffer, which is enough to get the beamformed data, is 37 mW. The total power consumption of the chip including the power consumption of the preamplifiers is 67 mW. The low power operation of this analog approach compared to the digital beamforming approaches using dedicated ADCs can be appreciated by noting the 270 mW power consumption of a single ADC system in [183] implemented in a similar 0.35-μm CMOS process for high-frequency ultrasound beamforming. If a dedicated ADC would be used for each channel the overall power consumption would be several times higher than 270 mW.

7.3.3. Advantages Compared to Other Analog-Filter-Based Delay Implementations

Various possible low-pass and all-pass filter implementations are investigated and compared for the analog delay generation. A major limitation of the use of low-pass filters for delay generation is the limited bandwidth. For instance, for 50-MHz operation, the delay dispersion allows a 1.25-ns delay per first-order low-pass filter, and a first-order low-pass filter [208] tuned to generate a 1.25-ns delay would have a 128-MHz bandwidth. When cascaded by 28 times (to achieve the required maximum delay of 35 ns

in this application), the cascaded bandwidth would drop to 20 MHz. Higher-order low-pass filters provide wider bandwidth for the same group delay. For instance, the bandwidth can be improved by 40% using a 2^{nd}-order low-pass filter with a Butterworth response. However, a 2^{nd}-order low-pass cell with a Butterworth response tuned for a 1.25-ns delay would have a 180-MHz bandwidth and when cascaded by 28 times the cascaded bandwidth would be 28 MHz, which is also less than the 50-MHz bandwidth requirement. The design in [209] uses a feed-forward path to introduce a zero to further improve the bandwidth and demonstrates a 50-MHz bandwidth in 0.7-µm BiCMOS when the designed delay cells are cascaded to generate a 20-ns delay. This implies that if the circuitry in [209] was used to achieve the 35-ns maximum delay needed in this application, its cascaded bandwidth would drop to less than 50 MHz. In addition, in the design in [209] the Butterworth response is controlled by the sizing of the transistors which does not allow post fabrication tuning. Furthermore, in these voltage mode approaches [208, 209] the delay-stage gain can be significantly different than unity. Even a 3^{rd}-order low-pass structure such as the one implemented on the work in [210] would have a 64-MHz bandwidth when it generates a 5-ns delay. When cascaded by 7 times (again for the required 35 ns total delay), the effective bandwidth would drop to below 50 MHz. In [211], a 4^{th}-order low-pass filter is developed that achieves a 26-ns delay with a 100-MHz bandwidth in 0.5-µm CMOS. This approach if tuned for a 35-ns delay would likely to meet the 50-MHz bandwidth target. However, implementation of the 4^{th}-order low pass circuitry is complex, power consuming and requires fine tuning circuits to tune the coefficients of the 4^{th}-order low-pass transfer function.

All-pass implementations have the bandwidth advantage over low-pass delay implementations because with an all-pass-based delay approach, the delay can be tuned to higher values without limiting the bandwidth. However, the all pass implementations in [212-214] are not well-suited for high-frequency applications because the finite bandwidth of the current or voltage amplifiers used in these techniques limit the frequency range over which the circuit behaves as an all-pass filter.

The all-pass delay circuitry in [215], which is also developed for ultrasound beamforming uses a log-domain low-pass filter to implement the all-pass function. The log domain approach combined with a class AB operation aimed to achieve a high linearity and low power approach, however the signal-dependent noise in this method is a concern for the image quality. In addition, in that design, the simple current mirror used for the signal inversion for the all-pass implementation limits the bandwidth of a single filter to 70 MHz.

The 2^{nd}-order all-pass filter implementation in [216] uses an inductor which is not typically provided in standard CMOS processes and in addition inductors consume a huge area. The work in [217] proposes an alternative 2^{nd}-order all-pass approach, which only uses capacitors and transistors in 0.35-µm SiGe. However, that approach suffers from reducing bandwidth for increased delay values. In addition, for a 10-ns delay it notes a 50-MHz bandwidth, which is not sufficient for this application.

Another all-pass-filter-based analog delay approach uses a collection of RC based delay cells for high-frequency annular arrays [124, 203, 218]. In this approach, the delay values can be adjusted by varying the R and C values. A drawback of this approach is that it requires a separate gain tuning voltage to compensate against the process variations

after fabrication to fine tune the all pass filter gain to one. It is worth noting that our current-mirror-based all-pass approach ensures a gain close to one without any external tuning. This is especially critical for a catheter-based application where the number of cables is limited. Moreover, this approach uses a differential delay cell and hence for a single-ended transducer it requires single-to-differential conversion at the input and differential-to-single ended conversion after the delay stages at the output. However, ultrasound transducers are inherently single ended devices and single-input single-output delay cells such as the one discussed in our work are hence more suitable for ultrasound application. Furthermore, although the approach is all-pass based, the bandwidth of the circuit is still limited by the bandwidth of the buffer circuit that drives the RC delay cell. Table 11 compares the performances of some of the analog delay approaches that are discussed in this section targeted for similar delay and frequency ranges.

Table 11. Performance comparison of some analog delay implementations in literature targeted for delay and frequency ranges comparable to this work

	[124]	[211]	[209]	[217]	This Work
Process	0.35-µm CMOS	0.5-µm BiCMOS	0.7-µm BiCMOS	0.35-µm SiGe	0.35-µm CMOS
Supply (V)	±3	5	5	3.3	3.3
Unit Delay Power (mW)	12	33	7.5	10.9	2.1
Unit Delay (ns)	0.86 - 2.4	3.5 – 5.0	1.67	1.0 – 5.0	1.75 - 2.5
Filter Type	1^{st} Order AP	4^{th} Order LP	1^{st} Order LP + 2^{nd} Order LP	2^{nd} Order AP	1^{st} Order AP
Bandwidth (MHz)	75 for 20 ns*	100 for 26 ns	50 for 20 ns	50 for 10 ns	150 for 35 ns

*Unit delay bandwidth is estimated as 250 MHz from the specified 0.1-dB gain dispersion in [124] between 42 – 58 MHz. The bandwidth in the table is projected assuming cascaded bandwidth of 8 first-order filters.

7.3.4. Current Preamplifier

For low noise amplification of the wideband CMUT current signal a variant of the capacitive-feedback-amplifier discussed in sections 2.3.4 and 4.2.2 is designed. The design is modified to create a current output instead of a voltage output (Figure 112). The current output of the amplifier enables direct addition of the signals in currents at the delay line nodes.

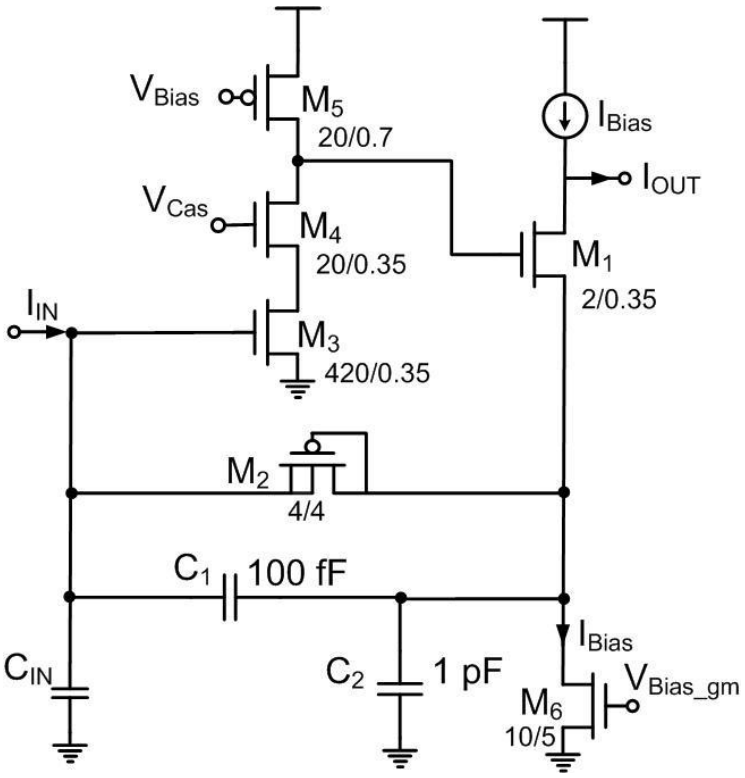


Figure 112. Schematic of the capacitive-feedback current amplifier used on the beamformer chip shown in Figure 105. Transistor sizes are shown in micrometers.

C_{IN} includes the CMUT capacitance, which is around 3 pF, and the parasitic capacitances. For CMUT-on-CMOS integration the parasitic capacitances can be neglected. Note that the size of the input transistor (M3) of the core amplifier is fairly large. This is done to minimize the voltage noise of the core amplifier which becomes dominant at the high operation frequencies of CMUT. I_{Bias} that flows on the drain of M1 is generated by mirroring the bias current generated by M6. Closely matching these two currents is critical because the unmatched current flows to the delay line and distorts its operation. The power consumption of the amplifier is 3.7 mW.

A test circuitry is designed to test the amplifier gain and bandwidth (Figure 113). An on-chip 20-kΩ poly-poly resistor is used to convert the input voltage to current. An

on-chip 3-pF mimics the capacitance of the annular-array CMUT element. Note that the same I-to-V converter that is shown in Figure 106 is used in this setup.

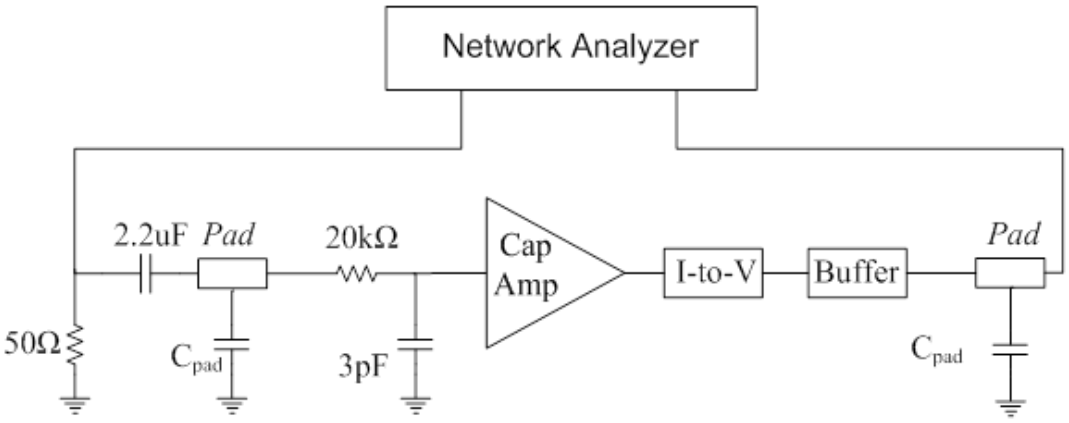


Figure 113. Setup for testing the amplifier gain and bandwidth

Figure 114 presents the measured transimpedance gain of the capacitive-feedback amplifier cascaded by the I-to-V converter. The measurement result demonstrates that the preamplifier has around 76 dB (6.3 kΩ) transimpedance gain with a bandwidth higher than 50 MHz. The drop at low frequencies (less than 3 MHz) is due to the high-pass pole generated by the 20-kΩ input resistance and the input capacitors and hence is a side-effect of the test setup. In simulations, the frequency response of the amplifier is flat at those low frequencies.

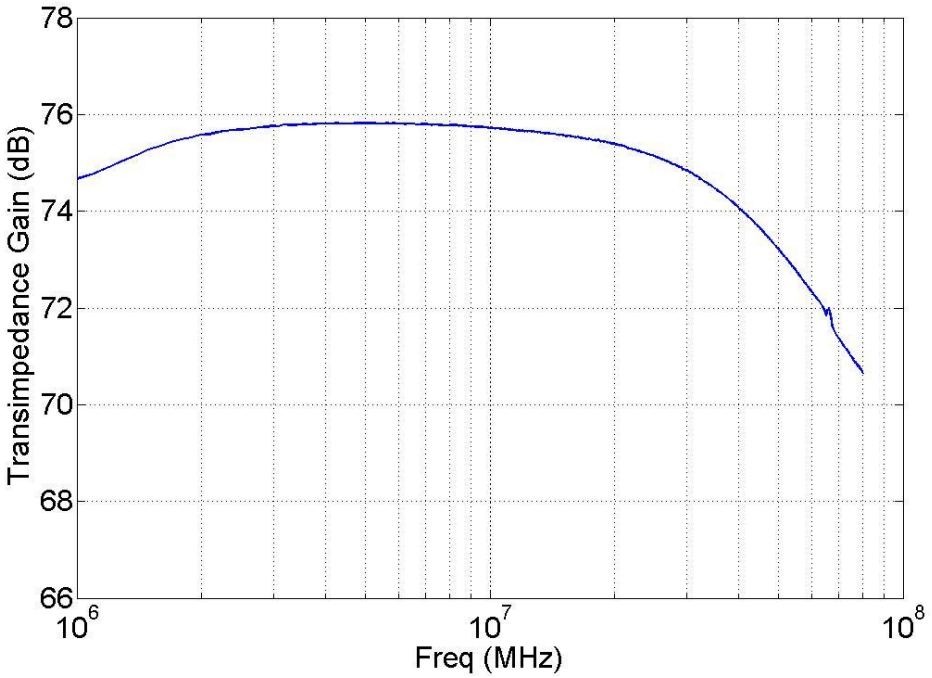


Figure 114. Transimpedance gain of the capacitive-feedback current amplifier cascaded with the I-to-V converter.

7.3.5. Experiment with Annular CMUT Array

For testing the beamformer IC with an actual transducer element, an 840-μm diameter CMUT annular array was wire bonded to a PCB. Although, the beamformer chip is designed for CMUT-on-CMOS integration, in this experiment an element of the CMUT array was connected to the beamformer test IC input by a cable. The parylene coated CMUT array was biased at 100-V dc and placed in a water tank for the experiments. One of the other CMUT array elements is used as a transmitter and is excited with a 10-ns pulse. Figure 115 plots the amplified CMUT pulse-echo signal before passing through the delay line (Out1) and after getting delayed through 14 delay cells, each with a 2-ns delay (Out8). The delayed waveform is scaled according to the gain of the delay line.

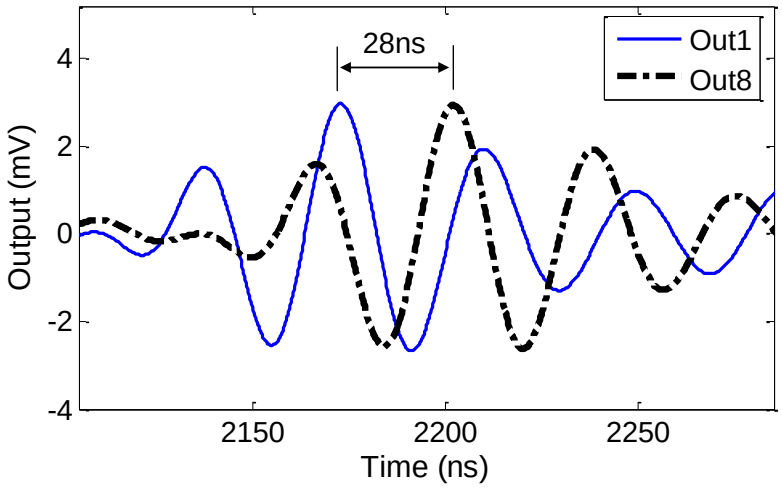


Figure 115. The detected CMUT pulse-echo signal (Out1) and the delayed waveform (Out8). The unit cell delay is 2 ns and the overall delay is 28 ns.

For an 840-μm diameter annular array, the delay range (1.75 ns to 2.5 ns) of the delay cell approximately corresponds to a range of focal distances from 1.4 mm (f#1.7) to 2.0 mm (f#2.4). It should be emphasized that, in the current design, for testing purposes all of the CMOS control voltages ($V_{Q\text{-}A,}$ $V_{Q\text{-}B}$, $V_{Cas\text{-}P}$, $V_{Cas\text{-}N}$ for delay cell; and V_{Bias}, $V_{Bias\text{-}gm}$, V_{Cas} for amplifier) are provided externally to the chip. However, it is possible to generate those voltages on chip. The only CMOS control voltage that needs to be provided and tuned externally is the delay tuning voltage ($V_{Tune\text{-}Delay}$).

7.4. Capacitive Delay Tuning

As discussed earlier, reducing the bias current to tune for higher delays reduces the dynamic range. In addition, since the output resistance of the current mirrors is large but finite, changing the bias current causes a slight gain change for different delay-tuning voltages. These can be improved by changing the delay tuning mechanism. Instead of modifying the bias current to tune the delay, alternatively, the loading capacitance at

node B-I (see Figure 97) can be adjusted either with a varactor or a capacitive bank controlled by switches.

A delay cell employing capacitive-delay tuning scheme is designed and simulated in 0.5-µm CMOS process (Figure 116). This design is modified from the delay cell design in Figure 97 and a capacitive bank controlled by switches is added. To characterize this delay cell a delay line consisting of 14 of these delay cells (similar to the delay lines that are discussed in the previous sections) is laid out and simulated. The capacitance values in the capacitance bank are chosen such that the unit delay can be tuned approximately between 1 ns and 2.5 ns in post layout simulations. The four control bits can be generated by an on-chip counter and since the delay values need to be reduced with increasing time (as shown in Figure 91) the counter should be a down-counter.

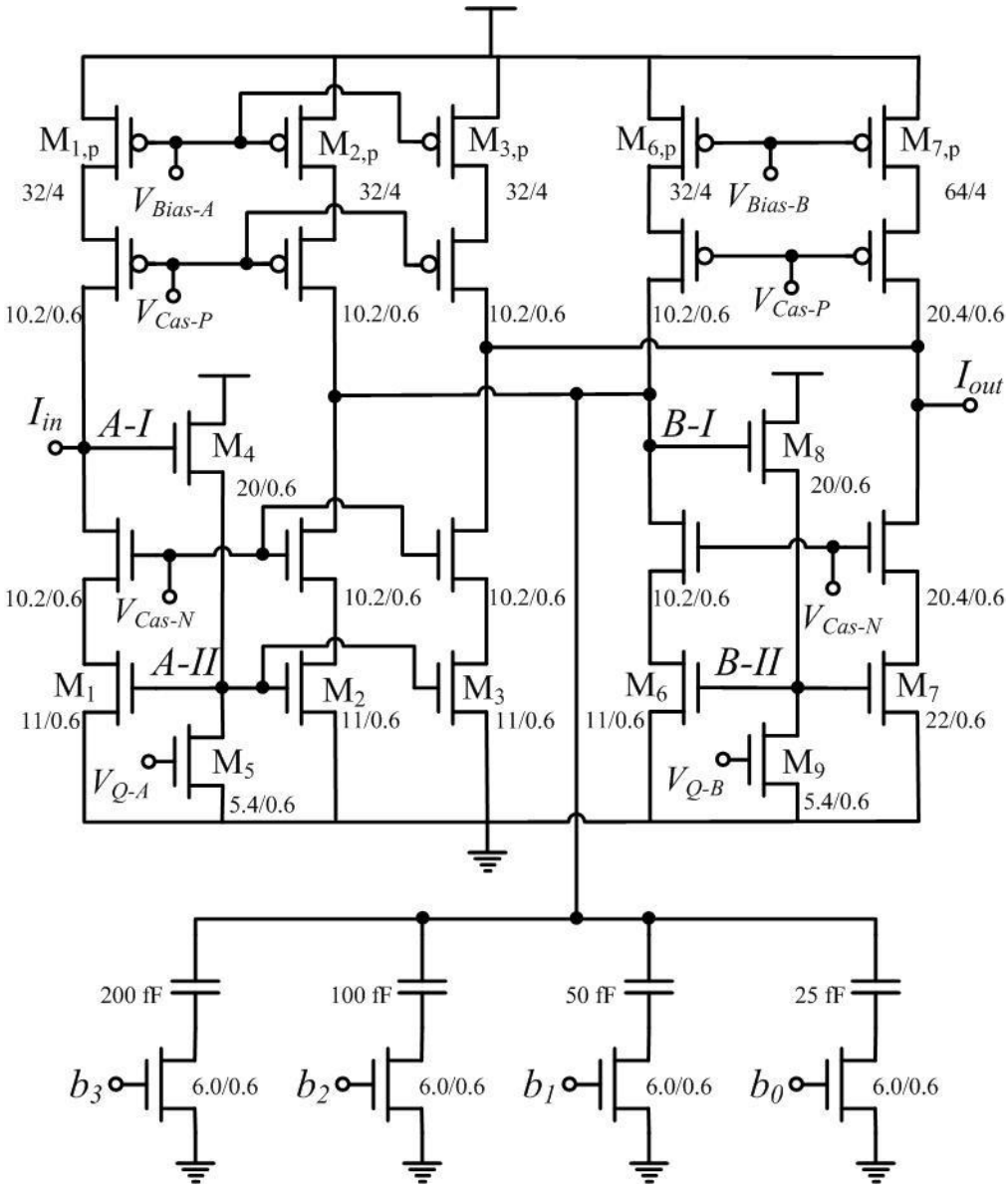


Figure 116. Schematic of the delay element with capacitive delay tuning using a capacitive bank controlled by 4 bits.

One concern of using a capacitive bank is that while switching the delay state some current gets injected to the delay line because of the charge leakage/clock feed through mechanisms. The injected switch current at each delay element accumulates along the delay line and the total current injection levels can become comparable to the

CMUT current levels. On the other hand, there are possible methods to minimize the impact of that switch current leakage.

A typical method to reduce the charge injection and clock feedthrough is to use dummy transistors with complementary clocks in the switches. Alternatively, the current injection of the switches can be negated to some extent by injecting a switching current with opposite polarity. In this application, this can partly be achieved by connecting a second switch array (with same-sized transistors) connecting very low value capacitors to the node labeled as A-I. The current injected by that switch array has opposite polarity compared to the leakage current injected by the switches on node B-I and therefore this can reduce the total injected current. This method is most effective in the case where "current multiplication by two" (which is required for the all-pass transfer function shown in (60)) function is implemented on the M2 branch instead of the M7 branch. This is possible because when the overall transfer function is concerned, there is no difference between implementing that "current multiplication by two" function using the M2 branch or the M7 branch. In that case, the switch current injected to node A-I has two routes to the output. The current gets multiplied by 2 in one route and multiplied by -1 in the other route and these cancel each other at the output effectively resulting in a multiplication with 1. On the other hand the current injected at node B-I gets multiplied by -1. Therefore, ideally at the output the injected currents cancel each other to totally eliminate the leakage effects at the output. However, in practice, the leakage currents does not completely cancel each other because the leakage current injected at node A-I gets delayed by some amount before adding to the node B-I and this prevents a complete

cancellation. Nevertheless, in simulations, using this method the current injection drops to less than 1/3rd of its regular values.

Another promising method to remove the effects of the leakage current from the data is to record the contribution of the switch current before the data collection and later subtract it from the collected data. Figure 117 shows simulation results showing various signals at the output of the delay line. Sim1 is the beamformed CMUT signal without any leakage current (i.e. the delay state was not changed during that timeframe). In Sim2 there is no CMUT signal and only the signals resulting from the switch leakage for two representative switching operations are shown. In Sim3, there is a CMUT signal at the time when the switch leakage is effective and thus the combination of both the CMUT signal and the switch leakage can be seen. The fourth plot demonstrates that it is possible to subtract the collected leakage without any data (Sim2) from the obtained data with leakage (Sim3) to extract back the clean CMUT signal. Note that this method is possible in this application because the injected switching current is not strongly dependent to the signal.

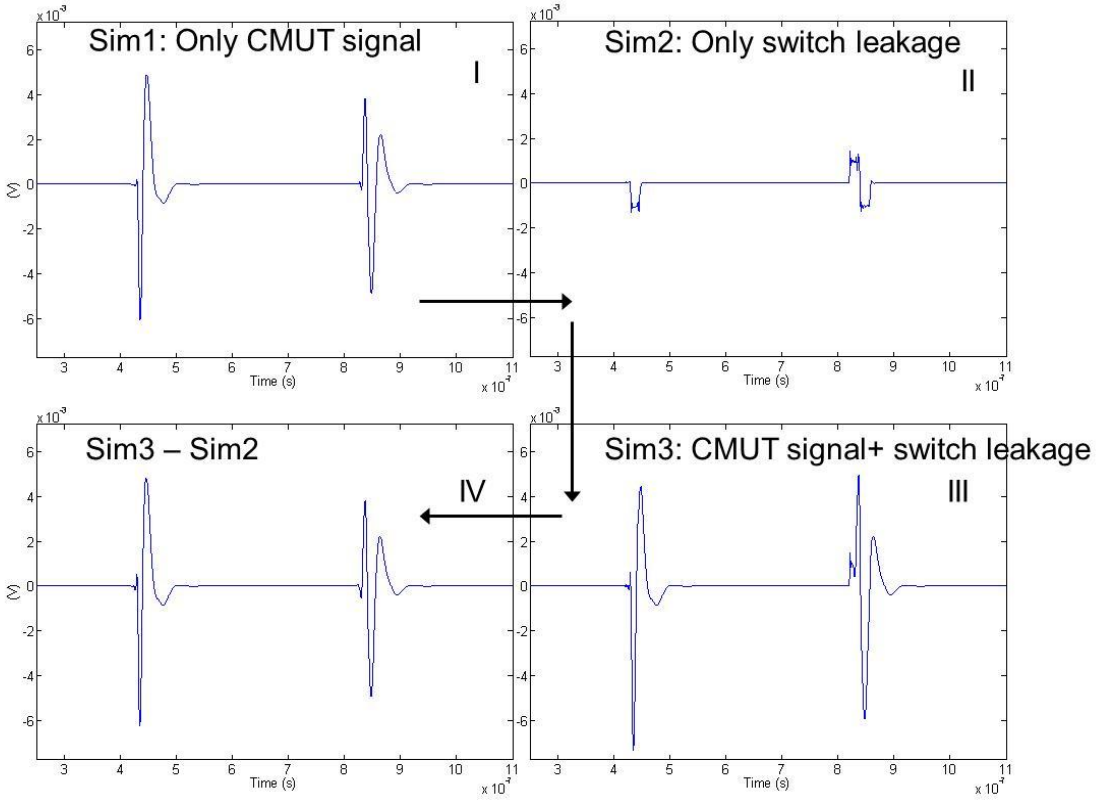


Figure 117. Simulation results using the delay cell in Figure 116 showing that the switch leakage current collected without any signal (II) can be subtracted from the collected data (III) to obtain a clear CMUT signal without any switching current (IV is very similar to I)

Table 12 shows the post-layout simulations results for delay and bandwidth values at the output of the delay line based on the delay cell shown in Figure 116. It can be seen that the total delay values for 14 delay cells can be tuned from 16.4 ns (1.2 ns per delay cell) to 36.5 ns (2.6 ns per delay cell) while maintaining a bandwidth higher than 200 MHz along the delay range. In addition, although it is not explicitly shown in Table 12, in post layout simulations the dynamic range of the delay line is found to be 45 dB throughout the whole delay range. As expected, the capacitive delay tuning enables to maintain a constant dynamic range within the delay range since the bias current is not reduced while tuning the delay.

Table 12. Post-layout simulation results for delay and bandwidth values at the output of the delay line containing 14 delay cells with capacitive delay tuning

Bits	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**
Delay (ns)	16.4	17.4	19.0	20.0	21.7	22.8	24.3	25.4
BW (MHz)	~530	~500	~440	~440	~330	~330	~330	~330
Bits	**1000**	**1001**	**1010**	**1011**	**1100**	**1101**	**1110**	**1111**
Delay (ns)	27.5	28.5	30.0	31.1	32.8	33.9	35.4	36.5
BW (MHz)	~200	~200	~200	~200	~200	~200	~200	~200

In Table 12, it can be seen that the bandwidth reduces for higher delay values, which happens because of the parasitic series resistance of the switches. The bandwidth reduction is dominated by the most significant bit since that connects the largest capacitor to the node. One design choice to reduce the resistance of the switches is related to the placement of the switches with respect to the capacitors. Note that in the schematic in Figure 116, the switches could be placed between the A-II node and the capacitors. However, instead the switches are placed between the capacitors and gnd because that gives a higher gate-to-source voltage when the switch is on compared to the other case and this reduces the on resistance.

Using a capacitive bank discretizes the implementable delay values. However, in practice that is not a concern because for each delay setting the receive beamformer need to maintain that delay setting until all the received echoes are processed and transferred to the beamformed output. For instance, for the high delay setting that fact requires to keep the delay state constant for around 35 ns. Nevertheless, if desired, the number of bits can

be increased to reduce the minimum delay increments. It should also be mentioned that in this section a capacitive bank approach is discussed. However, if a varactor with a low parasitic series resistor is provided by the design kit, then using that varactor is also a viable option for delay tuning.

7.5. Conclusion

A current-mode all-pass-filter-based analog delay cell that can generate variable delays at high frequencies is developed. This delay cell is designed to be used as the main building block in a delay line to apply proper delays to receive channels for dynamic receiver beamforming for a high-frequency ultrasound imaging system. A wideband biquad current mirror is explored as a tool to extend the bandwidth of the delay cell. This bandwidth enhancement method on the current mirrors used in the delay cell can improve the overall bandwidth of the delay line up to a factor of 6.

For the initial implementation of the delay approach, a receiver dynamic beamformer IC based on the developed delay cell is custom designed in 0.5-μm CMOS process. Each delay cell in this chip is measured to generate a tunable delay between 1.25 ns and 2.45 ns while keeping an almost constant group delay within a 50-MHz bandwidth. The delay line maintains a 60-MHz bandwidth for the highest delay setting and each delay cell consumes 7.5-mW at low delay setting and 3.3 mW at high delay setting. For the initial characterization of the beamforming system with the transducer array, this IC was integrated with a CMUT annular array. Preliminary focusing experiments demonstrated the delay variability on a single element as well as the beamforming capability of the approach.

The IC developed in 0.5-µm CMOS was designed for preliminary characterization of the beamforming approach and was not suitable for CMUT-on-CMOS integration. Based on the design approaches that are developed in the 0.5-µm CMOS chip, a beamformer IC that is suitable for monolithic integration with the CMUT array is designed in 0.35-µm CMOS. Measured results demonstrated that each delay cell is capable of generating a tunable delay between 1.75 ns to 2.5 ns, enabling dynamic receive beamforming over a focal range from f#1.7 to f#2.4. In addition, the measured bandwidth of the delay line is higher than 150 MHz for all the delay settings. Each delay cell consumes 2.1 mW and the power consumption of the whole IC is less than 70 mW. Thanks to its low power consumption, this IC is suitable for placement inside an IVUS catheter, unlike a digital beamforming approach based on multi-bit ADCs, which would be very cost inefficient and power consuming. The fabricated beamformer IC is integrated with an 8-element annular array. Experimental test results demonstrated the desired buffering, preamplification and delaying capabilities of the beamformer.

To improve the dynamic range limitation caused by the reduced bias current for high delay settings, a capacitive-delay-tuning method is developed. In post layout simulations, this method is demonstrated to achieve more than an octave tuning range with enough bandwidth and high dynamic range. One drawback of that approach is the noise generated during the switching action and to address that several methods that alleviate the effects of that injected switch current are discussed.

The wideband tunable delay circuitry that is developed and discussed in this chapter is not limited to use in IVUS in particular and its use can be extended to other applications that require wideband delay generation, such as equalizers. This delay

approach is also suitable for dynamic focusing in elevation to reduce the image slice thickness using 1.5-D ultrasound arrays.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1. Conclusions and Discussion of Technical Contributions

For intravascular ultrasound (IVUS) imaging catheters, close integration of front-end electronics and the transducer array within the catheter is highly desired because it reduces the cable count (by using multiplexing or beamforming) and enhances the system performance by mitigating the parasitic interconnect capacitances between the electronics and transducer array elements.

This research showed that it is possible to fit all of the required electronics in a single IC that can be integrated with the CMUT array using the CMUT-on-CMOS approach to realize a single-chip FL-IVUS system. The IC incorporates low-noise receiver amplifiers dedicated to each array element, 25-V pulsers, multiplexers, buffers and digital circuitry to synchronize the transmit and receive events. This single chip approach significantly mitigates the interconnection complexity and difficulties in the manufacturing of the IVUS probe. The overall system only requires 13 external cables in the catheter. The total power consumption of the IC is kept low enough (20 mW) to prevent over-heating of the device, which is critical since the device is located inside the human body. In addition, the whole chip fits into a very small (1.5-mm diameter) donut shaped area to be suitable for operation within a tiny vessel. Successful implementation of the single-chip FL-IVUS system is demonstrated through volumetric imaging experiments.

To achieve the required SNR levels from small CMUT elements, it is critical to custom design receiving electronics that leverage the advantages of the monolithic integration to minimize electronics noise for given bandwidth and element size specifications. In this research, a low-noise resistor-feedback TIA that is custom designed in the 0.35-μm CMOS process is demonstrated to have a 3-MΩ gain and 20-MHz bandwidth in a CMUT-on-CMOS implementation. The input-referred current noise of the designed TIA was measured as 90 fA/√Hz, which is less than the thermal-mechanical (T-M) noise of the CMUT element. In other words, with the results in this work, CMUT sensing is pushed to the limits of its sensitivity enabling to detect signals close to the T-M noise level of the CMUTs.

In addition to its direct advantage of maximized SNR, the transducer T-M noise dominated system can potentially enable new characterization, imaging and sensing applications. For instance, another important contribution of this work is that it showed that the relation between the CMUT impedance and the T-M noise spectrum of CMUT measured in air can be used as a simple, low power and passive means of characterizing the functionality and uniformity of the transducer array elements integrated with electronics.

The principles of the integration and circuit methods that are demonstrated in this dissertation for the development of the first fully-integrated single-chip FL-IVUS system can also be applied for realization of high-density 2D array systems where single-chip electronics integration is also very critical.

In parallel with the development of the single-chip FL-IVUS system effort, another application considered in this research that can also greatly benefit from close

electronics integration is high-frequency side-looking (SL) IVUS imaging with annular CMUT arrays. Currently, one of the main challenges that impede the realization of high-frequency catheter-based phased-array systems is the implementation of high-frequency beamforming circuitry inside the catheter in a power and area efficient manner. To address that challenge, a dynamic receive beamformer IC that is suitable for monolithic integration with an annular CMUT phased-array for SL-IVUS is custom designed in a 0.35-µm CMOS process. As the main building block in the beamformer IC, a current-mode all-pass-filter-based analog delay cell that can generate variable delays at high frequencies is developed. A biquad current mirror is explored as a method to extend the bandwidth of the delay cell. Measured results demonstrated that the beamformer IC is capable of implementing delays for dynamic receive beamforming over a focal range from f#1.7 to f#2.4. In addition, it is shown that the delay circuitry has a constant group delay and a flat magnitude response within the bandwidth of the transducer signal (30-50 MHz). Furthermore, the overall power consumption of the IC is kept small enough (~70 mW) for safe operation within a catheter. The fabricated beamformer IC was successfully connected to a CMUT annular array and experimental test results demonstrated the desired preamplification and receive beamforming capabilities of the IC.

In conclusion, this study is a unique demonstration of the integration of custom-designed electronics with an IC compatible transducer technology. Overall, the circuits and systems developed as part of this dissertation form a critical step in the translation of the research on CMUT-based IVUS catheters to enable next-generation imaging tools for better management of coronary arterial diseases.

8.2. Future Directions

8.2.1. Smart Power Management

As a means of failure protection and to enable higher power consumption while imaging, if needed, a low power integrated temperature sensing can be incorporated to the single-chip imaging device to protect the device against overheating. A circuit similar to the one proposed in [219] can be used to switch off the device at a predefined temperature. In this design, the MOS transistors are operated in subthreshold region, so the power consumption is kept as low as 10 μW. Inaccuracy in temperature threshold is less than 2°C and its layout consume only 0.04 mm^2. The temperature threshold can be set to about 42°C, so that if the imaging catheter is outside of the body and the temperature increases due to poor heat conduction (i.e. in dry conditions), the sensor will shut the system off. When inside the patient's body, the catheter will be operational and may consume more than 150 mW since blood is an effective heat sink. This capability can be explored as a possible way of using more active channels to improve frame rate or image quality.

8.2.2. Reducing the Size and the Number of External Connections for the Single-Chip FL-IVUS Device

Given that most CTO interventions are performed in arteries with 2.5 to 3-mm lumen size, the 1.5-mm diameter geometry of the FL-IVUS chip demonstrated in this work is reasonable. If needed though, the size of the device can be further reduced by squeezing the layout a little more. For instance by doing that, a 3.5F (1.17 mm) size catheter can be built. Naturally, this also requires careful packaging and electrical interconnect approaches. To further ease the manufacturing requirements, in future

designs, the number of external connections, which is 13 for the single-chip device presented in this work, can easily be reduced. The high-voltage supply for the pulser element (V_pulse_amp in Figure 59) and the two high-voltage dc biases for transmitter and receiver CMUT rings (V_Tx_bias and V_Rx_bias) can be provided through a single high-voltage source by using a low-power voltage-division method. The amplifier control voltages (Amp_ctrl1 and Amp_ctrl2) can be generated on-chip. Clear_ctr signal was useful for the electrical testing of the chip but it is not essential for the operation of the IC and therefore can be excluded from the final implementation. Therefore, the total number of required cables can be reduced to 8, which would only include the 4 output signals (Out1-to-4), vdd, gnd, the high-voltage line and clk.

8.2.3. An Alternative and More Compact Implementation of the Delay Cell

There is an alternative way of implementing the all-pass-based delay cell that realizes the transfer function given in (60) (Figure 118). The relative sizings of the transistors are shown in the figure. It can be seen that to maintain the improved bandwidth, this circuit also employs a biquad current mirror. The overall transfer function of the circuit in Figure 118 can be rewritten as

$$\frac{I_{out}}{I_{in}} = \frac{\dfrac{g_{m3,p}}{C_{A-I}}\dfrac{g_{m4,p}}{C_{A-II}}}{s^2 + s\dfrac{g_{m4,p}}{C_{A-II}} + \dfrac{g_{m3,p}}{C_{A-I}}\dfrac{g_{m4,p}}{C_{A-II}}}\frac{1 - sC_B/g_{m1}}{1 + sC_B/g_{m1}} \tag{73}$$

Similar to the design in Figure 107, the bandwidth of the circuit is controlled by the biquad containing nodes A-I and A-II; and the time constant at node B mainly tunes the delay of the cell. On the other hand, the delay cell shown in Figure 107 uses 24 transistors whereas the implementation in Figure 118 uses only 10 transistors. This

compact alternative looks attractive as it can reduce both the total noise and the current consumption of the delay line approximately to half compared to the delay line implementation based on the circuit shown in Figure 107.

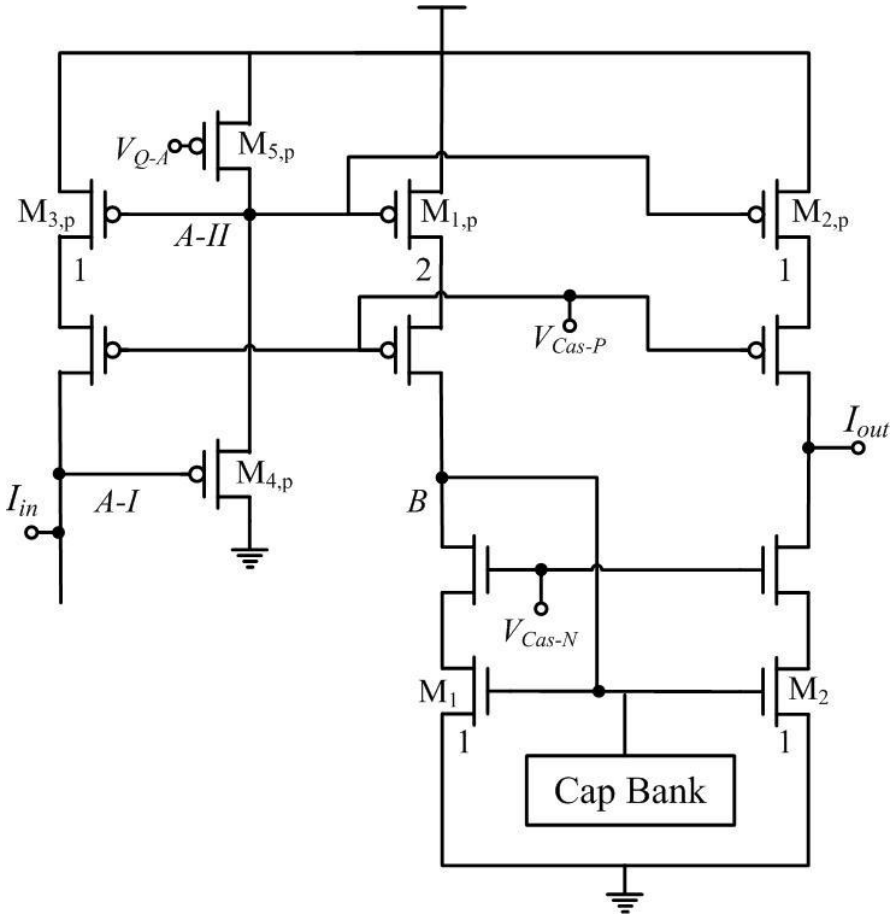


Figure 118. An alternative and more compact implementation of the first-order all-pass-based delay cell

When the delay cells in Figure 118 are cascaded in a delay line, each stage provides the bias current for the subsequent stage. The first delay cell of the delay line though should incorporate a circuit to generate the bias current, which gets transferred through the delay line. The dc points of nodes A-I and B should match closely for good current matching. Otherwise, the mismatched dc currents could get accumulated in the

delay chain. Maintaining the dc point matching for all the delay settings would not be possible if the delay was tuned with changing the bias current and therefore this approach is only feasible using a capacitive-delay-tuning method.

8.2.4. Post-Fabrication Calibration of the Delay

One can determine a mapping between the delay tuning settings and the delay value by using circuit simulations. However, analog integrated circuit implementations are susceptible to process, supply and temperature variations which causes the post fabrication delay values to be different than what the simulations predict. Therefore, after fabrication a testing routine must be performed to determine a correspondence table between the necessary delay control settings and the actual delay values. Alternatively, this manual post-fabrication calibration procedure can be eliminated by using an automated on-chip tuning mechanism. For instance, a frequency tuning loop such as the one proposed in [204] can be used to tune the delay of the all-pass element by using an off-chip reference signal. This approach uses a master - slave indirect tuning scheme to tune the cutoff frequency of the all-pass filter to precisely control the delay.

8.2.5. Transmit Beamforming and Pulsing Chip for SL-IVUS

One of the components needed for the final catheter implementation of the SL-IVUS system that is not discussed in detail in this dissertation is the TX IC, which is shown in Figure 104. This TX IC should incorporate high voltage pulsers and a digital delay circuitry to implement transmit beamforming. It should be noted that, implementation of transmit beamforming is relatively less challenging compared to receive beamforming because in transmit beamforming the signals to be delayed are

purely digital and conventional digital approaches can be used to accurately provide delayed pulse trigger signals to the high-voltage pulsers. On the other hand, receive beamforming needs to process analog signals. In addition, dynamic focusing is not applicable in transmit mode because once the ultrasound waves are created the transmit focal point is set and cannot be changed on the fly. On the other hand, it is possible to send successive pulses that are focused at different points along the image line. Therefore, in transmit mode, instead of dynamic focusing, few different focal points can be implemented, however with the trade-off of increased data acquisition time.

In [180], transmit beamforming delays are generated using discrete commercial parts, which is not a feasible approach for catheter-based applications because of the aforementioned cable number limitation that require the beamforming to be implemented with custom-designed ICs within the catheter. Some examples of digital-beamforming implementations based on custom-designed ICs for ultrasound applications can be seen in [52, 183, 220-222].

8.2.6. Improvements on the Transmit Power for FL-IVUS

In this work, the demonstrated 25-V peak-to-peak pulse amplitude is limited by the capabilities of the standard low-voltage CMOS technology. It is possible to use a more dedicated (but more expensive) 0.35-µm CMOS process that allows obtaining peak-to-peak pulse voltages up to 40-V, which is determined by the fundamental physical limitation of the devices in 0.35-µm CMOS technology. To further improve the pulse voltages, a high-voltage process with a much higher minimum feature size (i.e. the 0.8-µm CMOS technology in [103] enabling 300-V devices) can be used. The downside of doing that in a single-chip approach is that a technology with a higher minimum feature

size also increases the input capacitance values for the receive amplifier, which increases the system noise. In addition, with the increased minimum feature size, the receive circuitry would consume a larger area, which is a problem for an area starving application. One option might be to separate the high-voltage transmitter chip and the low noise receiver chips and to stack them vertically using TSVs. This seems like the ideal solution as it also preserves the compactness of the single-chip approach; however it complicates the integration process.

Another option to increase the transmit power without increasing the peak pulse voltages is to use coded excitation [223]. This approach uses a more sophisticated way of generating pulses to implement coding in the transmit waveform to improve the SNR. The trade-off is the need for a more complicated transmitter circuitry and some degradation in the axial resolution.

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